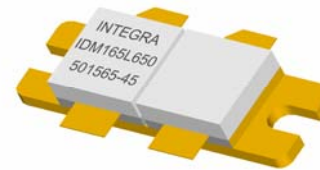


**VHF-Band Pulsed Power Transistor**

The high power pulsed transistor part number IDM165L650 is designed for VHF-Band systems operating at 125-167 MHz. Operating at a pulse width of 1ms with a duty factor of 20%, this dual MOSFET device supplies a minimum of 650 watts of peak pulse power at a fixed input power of 80 watts across the instantaneous operating bandwidth of 125-167 MHz. All devices are 100% screened for large signal RF parameters in the broadband RF test fixture across the entire specified operating bandwidth with no variable or external tuning.



**Silicon Bipolar**

- Ultra-high  $f_T$

**Class C Operation**

- High Efficiency

**Common Base Configuration**

- Single Power Supply

**Gold Metal**

- Maximum Reliability

**Emitter Ballasting**

- Optimum Thermal Distribution

**Internal Impedance Matching**

- Ease of Use
- Ultra-low Loss Design

**Be0 Package**

- Unmatched Thermal Reliability

**RF Test Fixture**

- Broadband
- Matched to 50Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning Allowed
- Micro-strip structure on soft pc board with dielectric constant 10.2

*TYPICAL DATA    TYPICAL DATA    TYPICAL DATA    TYPICAL DATA*

Device	Freq (MHz)	V <sub>CC</sub> (V)	P <sub>IN</sub> (W)	RL (dB)	P <sub>OUT</sub> (W)	G <sub>P</sub> (dB)	I <sub>C</sub> (A)	η <sub>C</sub> (%)	Droop (dB)	Pout @ Pin+1dB
1273-16	125	34	80	14	763	9.8	35.0	64	-0.39	813
	146	34	80	21	689	9.5	32.7	62	-0.40	718
	167	34	80	12	660	9.2	31.0	63	-0.38	729

Pulse Format = 1ms, 20%

**MAXIMUM RATINGS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	$V_{DS}$	--	80	V	--
BD	Emitter-Base Voltage	$V_{GS}$	--	20	V	--
BD	Storage Temperature Range	$T_{STG}$	-55	+150	°C	--
BD	Operating Junction Temperature Range	$T_J$	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

**THERMAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.25	°C/W	$V_{DD}=V1, I_{DQ}=0mA, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=650W.$
Note	Screen 'BD' = parameter qualified By Design.					

**PROCESSING SPECIFICATIONS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification.
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

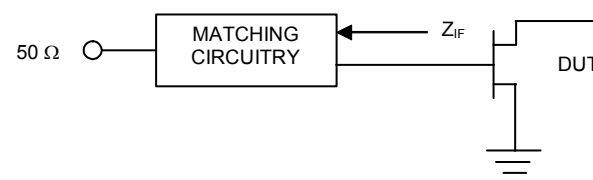
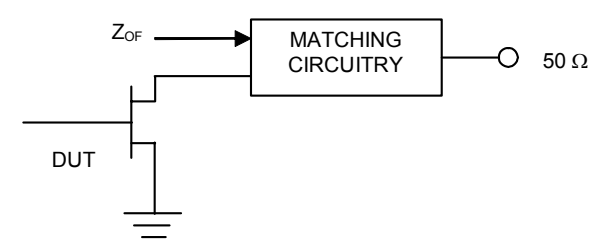
**DC ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage (each side)	$BV_{DSS}$	80	--	V	$I_D=50mA, V_{GS}=0V, T_F=25\pm5^\circ C.$
100%	Drain Leakage Current (each side)	$I_{DSS}$	--	5	mA	$V_{DS}=34V, V_{GS}=0V, T_F=25\pm5^\circ C.$
100%	Gate Threshold Voltage 1 (each side)	$V_{Gsth1}$	1.0	--	V	$I_D=100\mu A, V_{GS}=10V, T_F=25\pm5^\circ C.$
100%	Gate Threshold Voltage 2 (each side)	$V_{Gsth2}$	2.0	--	V	$I_D=50mA, V_{GS}=10V, T_F=25\pm5^\circ C.$

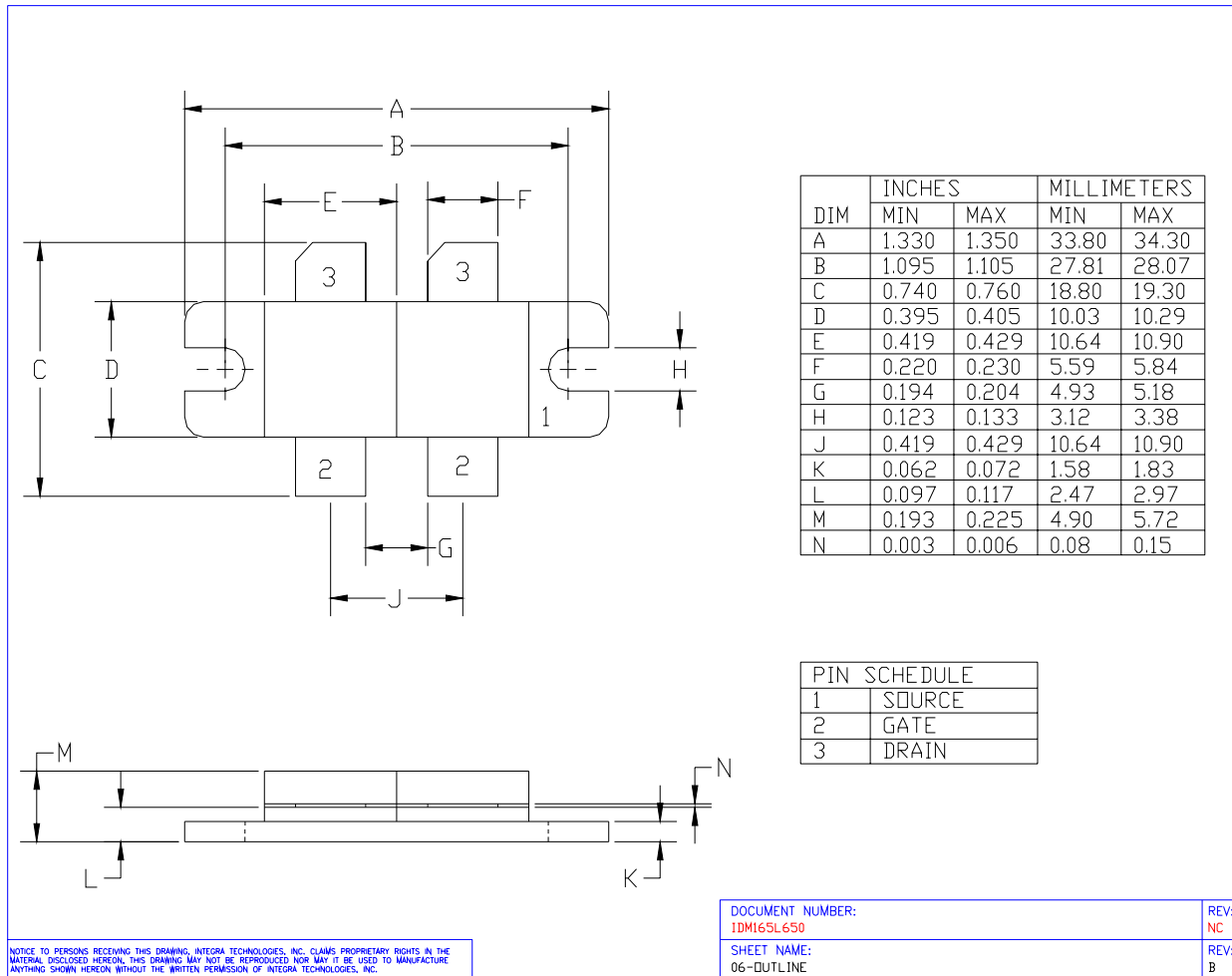
**RF ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	10	--	dB	$V_{DD}=V1, I_{DQ}=0mA, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Output Power	$P_O$	650	--	W	$V_{DD}=V1, I_{DQ}=0mA, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Drain Efficiency ( $P_O/I_D/V_{DD}$ )	$N_D$	40	--	%	$V_{DD}=V1, I_{DQ}=0mA, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Pulse Amplitude Droop	D	--	1.0	dB	$V_{DD}=V1, I_{DQ}=0mA, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1, F2, F3.$ Measure between 100us and 900us time positions.
100%	Power Gain	$G_P$	9.1	--	dB	$V_{DD}=V1, I_{DQ}=0mA, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Gain Flatness versus Frequency	GF	--	1.2	dB	$GF = MAX(G_P) - MIN(G_P).$
100%	Stability into 2:1 VSWR	VSWR-S	S	--	--	$V_{DD}=V1, I_{DQ}=0mA, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1, F2, F3.$ Rotate 2:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
100%	3:1 Load Mismatch Tolerance	LMT	P	--	--	$V_{DD}=V1, I_{DQ}=0mA, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1, F2, F3.$ Rotate 3:1 output VSWR through 360° phase. Post test $P_O = \text{Pre test } P_O \pm 10W.$
100%	Overdrive Stability	OD-S	S	--	--	$V_{DD}=V1, I_{DQ}=0mA, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1, F2, F3.$ No oscillatory or pulse break-up characteristics allowed on detected output pulse.
Note	$V1 = 34V; PW1 = 1ms; DF1 = 20%; P_{IN1} = 80W; P_{IN2} = 100W; F1 = 125MHz, F2 = 146MHz, F3 = 167MHz.$					
Note	$T_F = \text{Device flange temperature.}$					

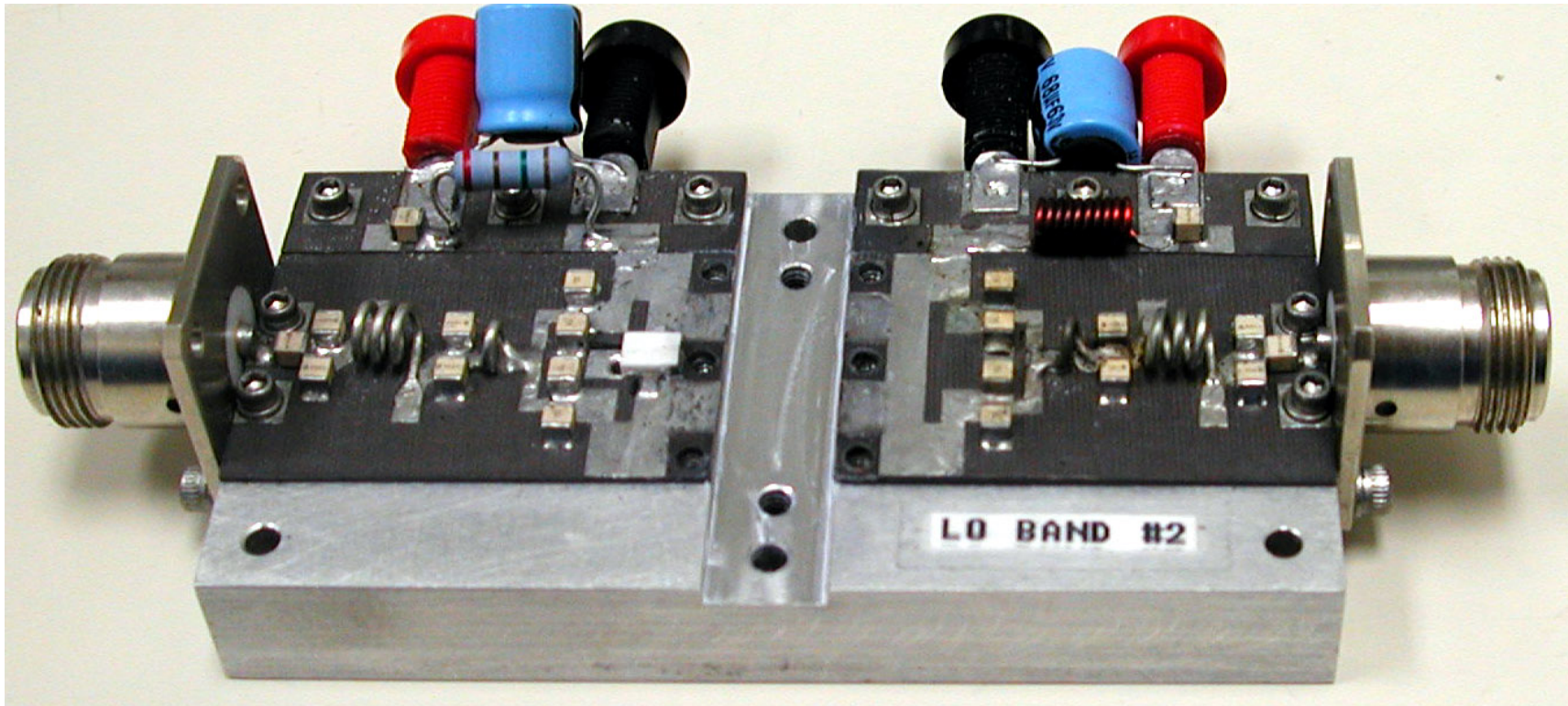
**BROADBAND RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

Frequency (MHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
125	1.558 + j0.013	1.632 + j0.035
146	1.565 + j0.157	1.760 + j0.105
167	1.248 + j0.698	1.415 + j0.484
Impedance Definition		

**PACKAGE DIMENSIONAL OUTLINE DRAWING**



**BROADBAND RF TEST FIXTURE**



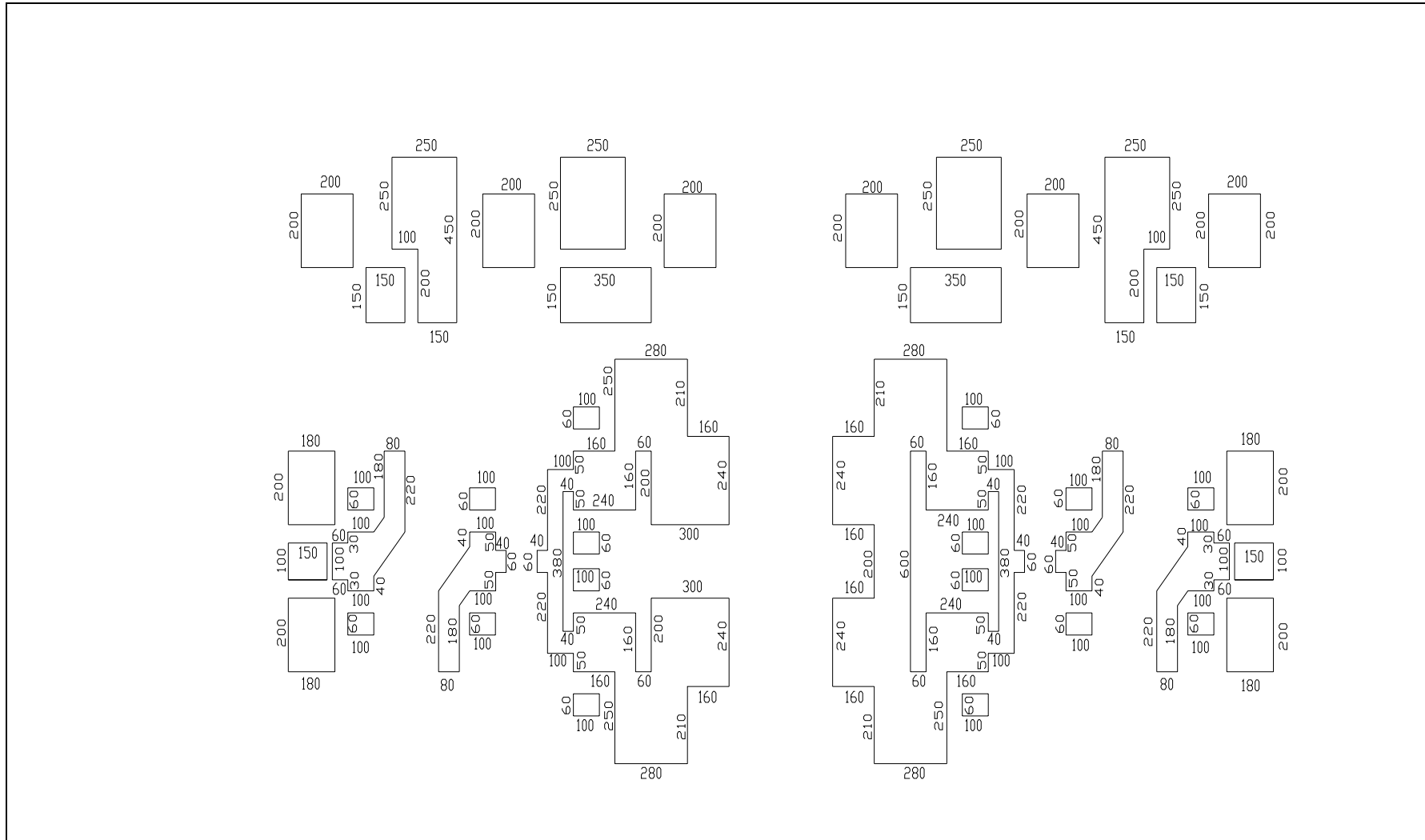
PHOTOGRAPH

**BROADBAND RF TEST FIXTURE**



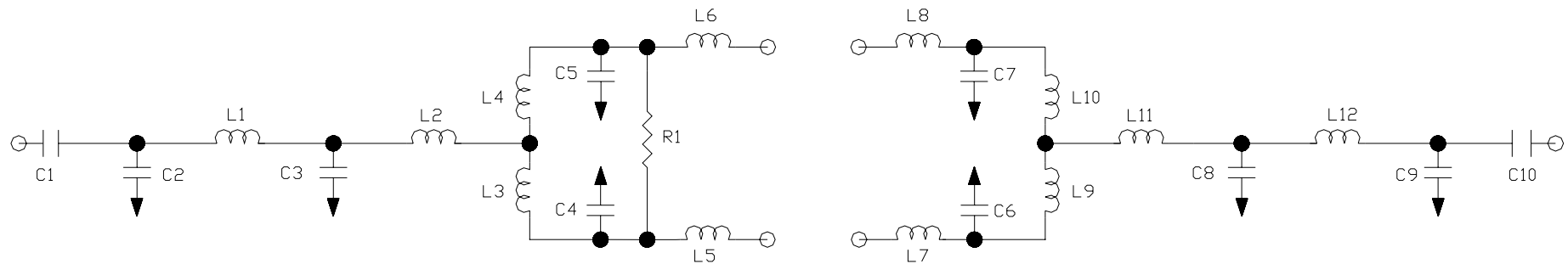
ASSEMBLY AND PARTS LIST

**BROADBAND RF TEST FIXTURE**



**CIRCUIT DIMENSIONS**

**BROADBAND RF TEST FIXTURE**



ELECTRICAL SCHEMATIC



**DEFINITIONS**

<b>Data Sheet Status</b>	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
<b>Maximum Ratings</b>	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

**WARNING**

<b>Product and environmental safety - toxic materials</b>
This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

**DISCLAIMER**

Integra Technologies Inc. reserves the right to make changes without further notice to any products herein. Integra Technologies Inc. makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Integra Technologies Inc. assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Integra Technologies Inc. products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Integra Technologies Inc. customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Integra Technologies Inc. for any damages resulting from such improper use or sale.
------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------