

Avionics Band RF Power LDMOS FET

The high power transistor part number ILD0912M150HV is designed for Avionics systems operating at 960-1215 MHz. Operating at 10 μ s, 10% pulse conditions this LDMOS FET device supplies a minimum of 150 watts of power across the instantaneous operating bandwidth of 960-1215 MHz. All devices are 100% screened for large signal RF parameters.



Silicon LDMOS FET

- High Power Gain
- Superior thermal stability

Class AB Operation

- Gate biased to $I_{DQ} = 10 \text{ mA}$

Configuration

- Common Source

Gold Metal

- Maximum Reliability

Package

- Thermally enhanced
- Pb-free and RoHS-compliant

Epoxy Sealed Lid

- Gross Leak Qualified

RF Test Fixture

- Broadband
- Matched to 50 ohms
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

TYPICAL DATA

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| Freq (MHz) | P_I (W) | I_{dr} | I_d (A) | RL (dB) | P_O (W) | N_d (%) | N_d' (%) | G (dB) | Droop (dB) | VSWR | |
|---------------|--------------|----------|--------------|------------|--------------|--------------|---------------|-----------|---------------|------|------|
| | | | | | | | | | | 2:1 | 20:1 |
| 960 | 8 | 0.626 | 6.26 | 11.6 | 184 | 58.8 | 59.7 | 13.62 | 0.02 | S | P |
| 1090 | 8 | 0.724 | 7.24 | 12.4 | 196 | 54.1 | 54.9 | 13.89 | 0.02 | S | P |
| 1215 | 8 | 0.629 | 6.29 | 13 | 170 | 54.1 | 54.9 | 13.27 | 0.00 | S | P |

Pulse format = 10 μ s, 10%, $I_{DQ} = 10\text{mA}$

N_d = Drain efficiency (including bias current)

N_d' = Drain efficiency (excluding bias current)

MAXIMUM RATINGS

| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|--------|--|-----------|-----|------|-------|-----------------|
| BD | Drain-Source Voltage | V_{DS} | -- | 70 | V | -- |
| BD | Gate-Source Voltage | V_{GS} | -- | 20 | V | -- |
| BD | Storage Temperature Range | T_{STG} | -55 | +200 | °C | -- |
| BD | Operating Junction Temperature Range | T_J | -55 | +200 | °C | -- |
| Note | Screen 'BD' = parameter qualified By Design. | | | | | |

THERMAL CHARACTERISTICS

| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|--------|--|--------------|-----|-------|-------|---|
| BD | Thermal Resistance | $R_{TH(JC)}$ | -- | 0.070 | °C/W | $V_D=50V, I_{DQ}=10mA, T_F=25\pm 5^\circ C, P_{OUT}=150W$ |
| Note | Screen 'BD' = parameter qualified By Design. | | | | | |

PROCESSING SPECIFICATIONS

| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|--------|--|--------|-----|-----|-------|---|
| 100% | DC Wafer Probe | -- | -- | -- | -- | Per Integra specification. |
| Q1 | Wafer DC and RF Qualification | -- | -- | -- | -- | Per Integra specification. |
| LM | Wire Bond Strength | -- | -- | -- | -- | Line monitor per Integra specification. |
| 100% | Pre-cap visual inspection | -- | -- | -- | -- | Per Integra specification |
| 100% | Gross leak test | -- | -- | -- | -- | MIL-STD-750D, Method 1071, Test Condition C |
| Note | Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer. | | | | | |
| Note | Screen 'LM' = parameter is qualified by assembly line monitor. | | | | | |

DC ELECTRICAL CHARACTERISTICS

| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|--------|--------------------------------|------------|-----|-----|---------|--|
| 100% | Drain-Source Breakdown Voltage | BV_{DSS} | 100 | | V | $I_D = 10mA, V_{GS} = 0V, T_F = 25\pm 5^\circ C$ |
| 100% | Drain Leakage Current | I_{DSS} | | 1 | μA | $V_{DS} = 50V, V_{GS} = 0V, T_F = 25\pm 5^\circ C$ |
| 100% | Gate Threshold Voltage | V_{GS} | 2.0 | 4.0 | V | $I_D = 10mA, T_F = 25\pm 5^\circ C, V_{DS} = 5V$ |

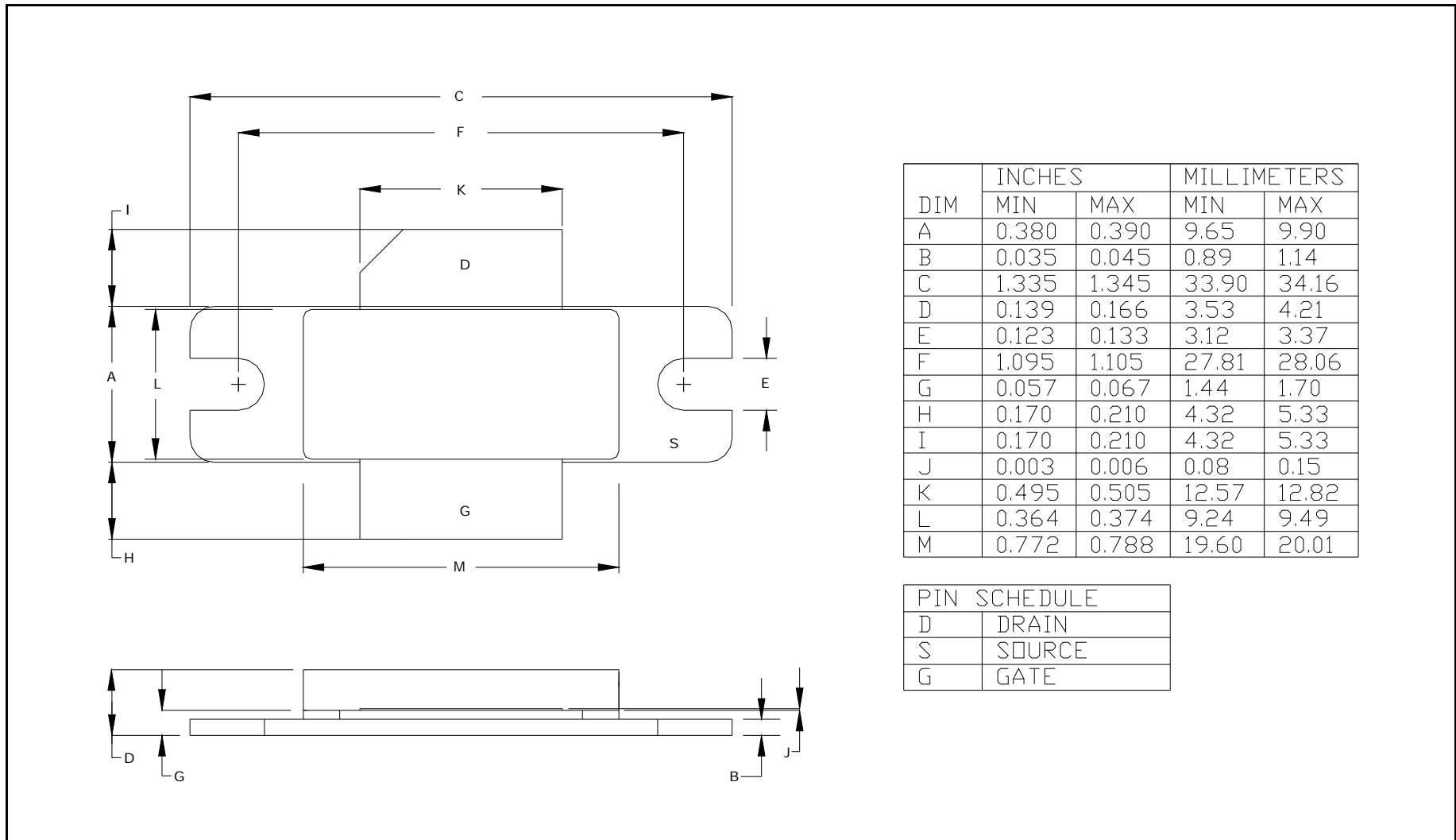
RF ELECTRICAL CHARACTERISTICS

| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|--------|--|---------------|-------|-------|-------|---|
| 100% | Input Return Loss | IRL | -18 | -9 | dB | $V_{DD}=50V, P_{IN}=8W, \text{Pulse}=10\mu s, 10\%, T_F=25\pm 5^\circ C, F=F1, F2, F3, I_{DQ}=10mA.$ |
| BD | Maximum Overdrive | $P_{IN(MAX)}$ | 12 | | W | $V_{DD}=50V, \text{Pulse}=10\mu s, 10\%, T_F=25\pm 5^\circ C, F=F1, F2, F3, I_{DQ}=10Ma.$ |
| 100% | Power Gain | G_P | 12.73 | 14.23 | dB | $V_{DD}=50V, P_{IN}=8W, \text{Pulse}=10\mu s, 10\%, T_F=25\pm 5^\circ C, F=F1, F2, F3, I_{DQ}=10mA.$ |
| 100% | Output Power | P_{OUT} | 150 | 212 | W | $V_{DD}=50V, P_{IN}=8W, \text{Pulse}=10\mu s, 10\%, T_F=25\pm 5^\circ C, F=F1, F2, F3, I_{DQ}=10mA.$ |
| 100% | Drain Efficiency | N_d' | 50 | 75 | % | $V_{DD}=50V, P_{IN}=8W, \text{Pulse}=10\mu s, 10\%, T_F=25\pm 5^\circ C, F=F1, F2, F3, I_{DQ}=10mA.$ |
| 100% | Pulse Amplitude Droop | D | -0.50 | +0.50 | dB | $V_{DD}=50V, P_{IN}=8W, \text{Pulse}=10\mu s, 10\%, T_F=25\pm 5^\circ C, F=F1, F2, F3, I_{DQ}=10mA.$ |
| 100% | Stability into 2:1 VSWR | VSWR-S | | | -- | $V_{DD}=50V, P_{IN}=8W, \text{Pulse}=10\mu s, 10\%, T_F=25\pm 5^\circ C, F=F1, F2, F3, I_{DQ}=10mA.$ Rotate 2:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. |
| BD | Load Mismatch Tolerance | LMT | | 20:1 | -- | $V_{DD}=50V, P_{IN}=8W, \text{Pulse}=10\mu s, 10\%, T_F=25\pm 5^\circ C, F=F1, F2, F3, I_{DQ}=10mA.$ Rotate 20:1 output VSWR through 360° phase. Survival. |
| BD | Pulse Risetime | RT | | 60 | ns | $V_{DD}=50V, P_{IN}=8W, \text{Pulse}=10\mu s, 10\%, T_F=25\pm 5^\circ C, F=F1, F2, F3, I_{DQ}=10mA.$ Measure between 10% and 90% detected power points. |
| Note 1 | F1 =960 MHz, F2=1090MHz, F3=1215MHz. | | | | | |
| Note 2 | Pulse format = 10μs, 10% | | | | | |
| Note 3 | T_F = Device flange temperature. | | | | | |
| Note 4 | Screen 'BD' = parameter qualified By Design. | | | | | |

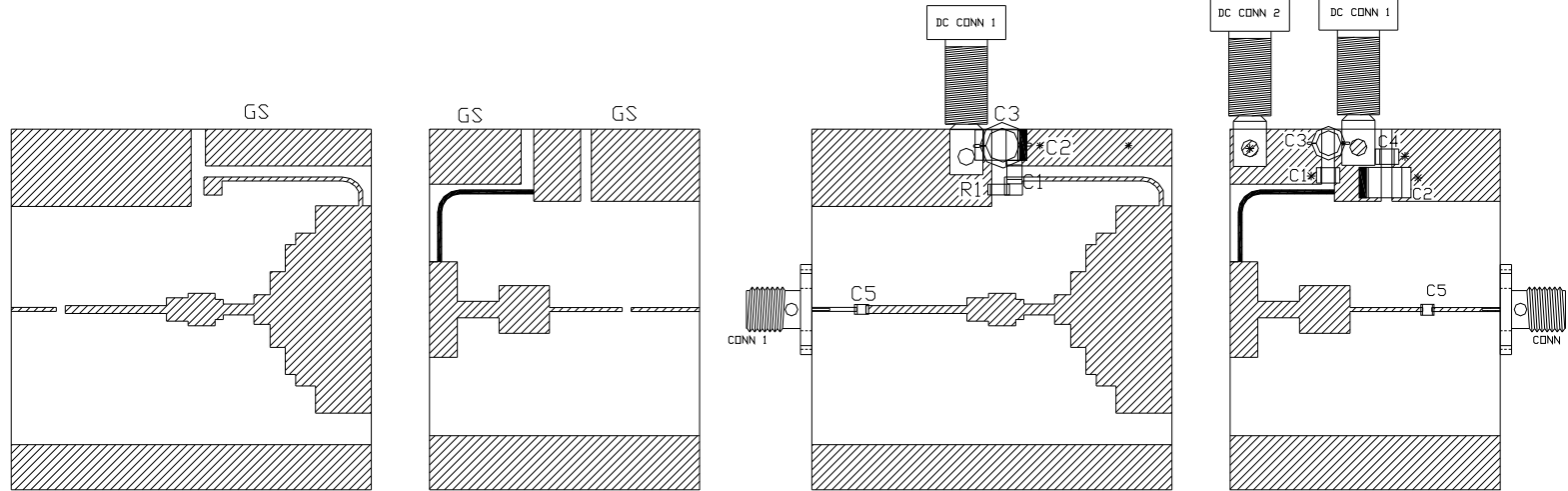
RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

| Frequency (MHz) | $Z_{IF} (\Omega)$ | $Z_{OF} (\Omega)$ |
|----------------------|-------------------|-------------------|
| 960 | 1.15 -j0.82 | 3.70 -j3.86 |
| 1090 | 1.10 -j0.52 | 3.50 -j2.20 |
| 1215 | 0.83 -j0.21 | 3.62 -j0.70 |
| Impedance Definition | | |

PACKAGE DIMENSIONAL OUTLINE DRAWING

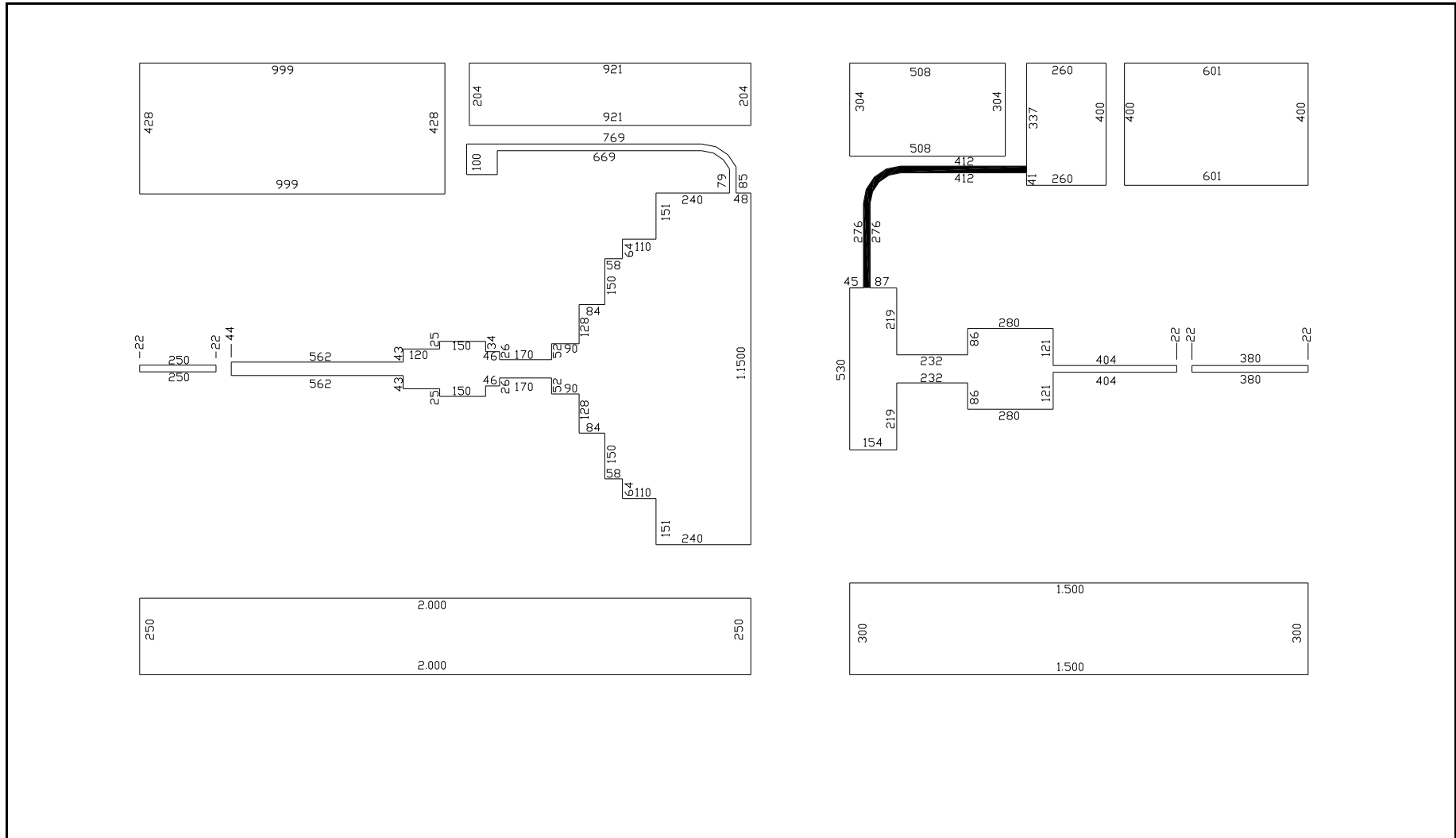


RF TEST FIXTURE – ASSEMBLY AND PARTS LIST

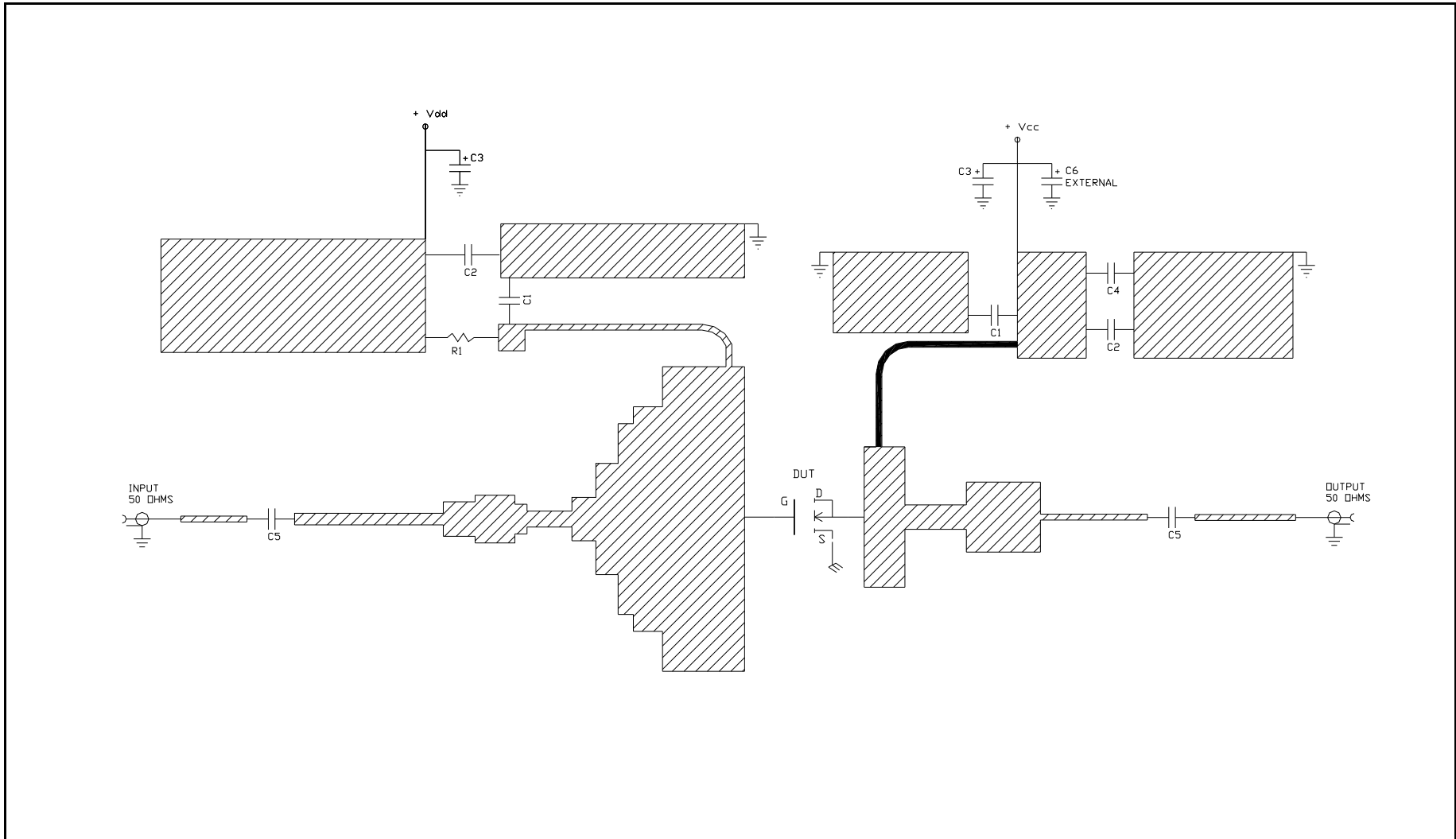


| COMPONENT | DESCRIPTION |
|-------------------------|--|
| DUT | TRANSISTOR ILD0912M150HVX MOUNT HARD TO THE RIGHT |
| PC BOARD | RODGERS #R0 3010 10.2" .025" 1oz Cu |
| C1 | CHIP CAPACITOR ATC100B-47pF (2PLCS) |
| C2 | TANTALUM - AVX 4.7 uF, 50V ESR = 0.3OHMS (2PLCS) |
| C3 | ELECTROLYTIC CAPACITOR 68uF/63V |
| C4 | CHIP CAPACITOR CERAMIC ATC100B - 1000pF 250V |
| C5 | CHIP CAPACITOR ATC100A - 39 pF (2PLCS) |
| C6 (NOT SHOWN) | ELECTROLYTIC CAPACITOR: 4700uF / 50V |
| R1 | RESISTOR 120g - 300 OHMS |
| GS (6 PLACES) | GROUND SHIM, COPPER, TH=0.001" |
| CONN 1, CONN 2 | SMA CONNECTOR, DS #2052-5636-02 |
| INPUT PC BOARD CARRIER | 2 INCH BRASS-07 (2.0") |
| OUTPUT PC BOARD CARRIER | 2 INCH BRASS-05 (1.5") |
| TRANSISTOR CARRIER | 2 INCH COPPER-22 |
| TRANSISTOR CLAMP | NDRYL CLAMP-08 |
| ALUMINUM HEAT SINK | 2 INCH HEATSINK-11 |
| DC CONN 1 | BANANA JACK, BLACK |
| DC CONN 2 | BANANA JACK, RED |
| NOTE | USE CORNELL DUBLIER ALUMINUM FLAT PACK *MLP* SERIES OR SIMILAR FOR STORAGE CAPACITOR FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST |

RF TEST FIXTURE – CIRCUIT DIMENSIONS IN MILS



RF TEST FIXTURE – ELECTRICAL SCHEMATIC



DEFINITIONS

| Data Sheet Status | |
|---|---|
| Proposed Specification | This data sheet contains proposed specifications. |
| Preliminary Specification | This data sheet contains specifications based on preliminary measurements and data. |
| Product Specification | This data sheet contains final product specifications. |
| Maximum Ratings | |
| Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability. | |

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