

## Avionics Band RF Power LDMOS FET

The high power transistor part number ILD1011M275HV is designed for Avionics systems operating at 1030-1090 MHz. Operating at 50µs, 2% pulse conditions this LDMOS FET device supplies a minimum of 275 watts of power at 1030/1090 MHz. All devices are 100% screened for large signal RF parameters.



### Silicon LDMOS FET

- High Power Gain
- Superior thermal stability

### Class AB Operation

- Gate biased to  $I_{DQ} = 10 \text{ mA}$

### Configuration

- Common Source

### Gold Metal

- Maximum Reliability

### Package

- Thermally enhanced
- Pb-free and RoHS-compliant

### Epoxy Sealed Lid

- Gross Leak Qualified

### RF Test Fixture

- Broadband
- Matched to 50 ohms
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

## TYPICAL DATA    TYPICAL DATA    TYPICAL DATA    TYPICAL DATA

Devices	Freq (GHz)	PW (us)	Duty (%)	Vcc (V)	P <sub>IN</sub> (W)	IRL (dB)	Pout (W)	Gp (dB)	Id (A)	Nd (%)	Droop (dB)	VSWR	
												3:1	20:1
D5086-2	1.030	50	2	50	10.0	14.00	306	14.9	13.10	46.7	-0.028	S	P
	1.090	50	2	50	10.0	15.00	328	15.2	12.50	52.5	-0.094	S	P

**MAXIMUM RATINGS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	$V_{DS}$	--	70	V	--
BD	Gate-Source Voltage	$V_{GS}$	--	20	V	--
BD	Storage Temperature Range	$T_{STG}$	-55	+200	°C	--
BD	Operating Junction Temperature Range	$T_J$	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

**THERMAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.034	°C/W	$V_D=50V, I_{DQ}=20mA, T_F=25\pm 5^\circ C, P_{OUT}=275W$
Note	Screen 'BD' = parameter qualified By Design.					

**PROCESSING SPECIFICATIONS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

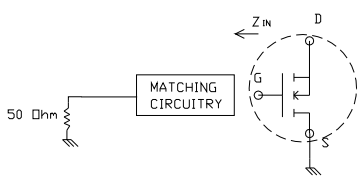
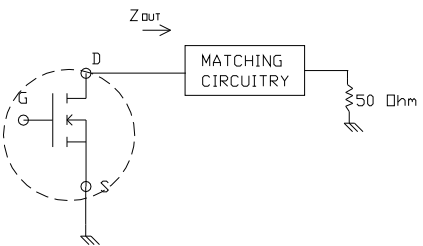
**DC ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	$BV_{DSS}$	100		V	$I_D = 20mA, V_{GS} = 0V, T_F = 25\pm 5^\circ C$
100%	Drain Leakage Current	$I_{DSS}$		10	$\mu A$	$V_{DS} = 50V, V_{GS} = 0V, T_F = 25\pm 5^\circ C$
100%	Gate Threshold Voltage	$V_{GSTH2}$	2.5	10	V	$I_D = 20mA, T_F = 25\pm 5^\circ C, V_{DS} = 5V$

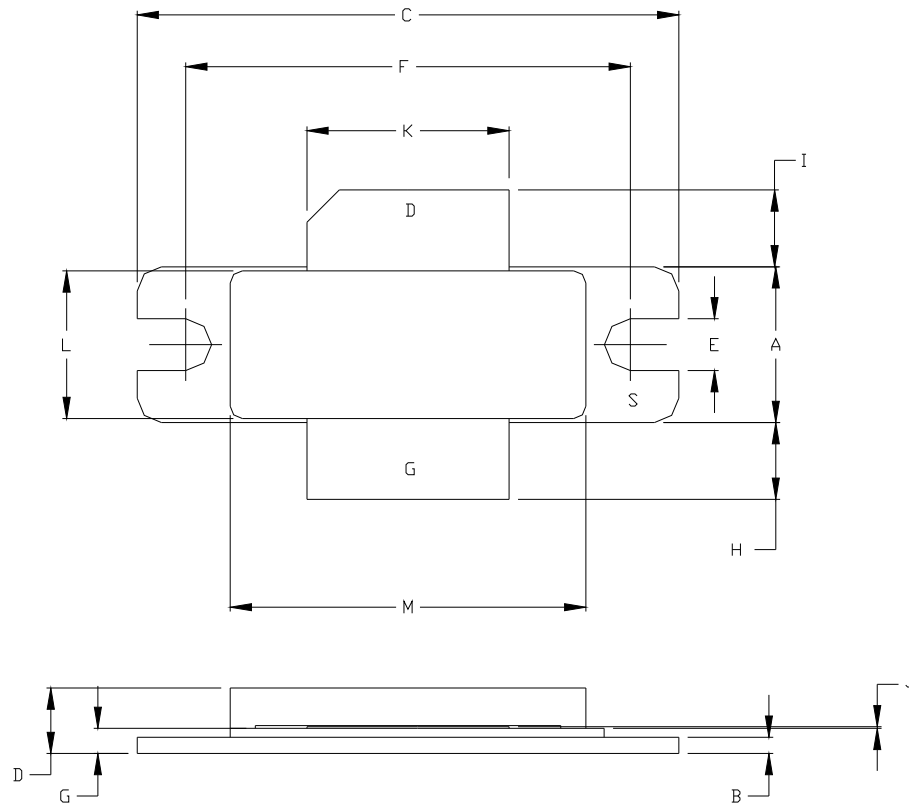
**RF ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-10	dB	$V_{DD}=50V$ , $P_{IN}=10W$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , $F=F1, F2$ , $I_{DQ}=20mA$ .
BD	Maximum Overdrive	$P_{IN(MAX)}$		14	W	$V_{DD}=50V$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , $F=F1, F2$ , $I_{DQ}=20mA$ .
100%	Power Gain	$G_P$	14.4	15.9	dB	$V_{DD}=50V$ , $P_{IN}=10W$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , $F=F1, F2$ , $I_{DQ}=20mA$ .
100%	Output Power	$P_{OUT}$	275	388	W	$V_{DD}=50V$ , $P_{IN}=10W$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , $F=F1, F2$ , $I_{DQ}=20mA$ .
100%	Drain Efficiency	$N_D$	40	--	%	$V_{DD}=50V$ , $P_{IN}=10W$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , $F=F1, F2$ , $I_{DQ}=20mA$ .
100%	Pulse Amplitude Droop	D	-0.5	0.5	dB	$V_{DD}=50V$ , $P_{IN}=10W$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , $F=F1, F2$ , $I_{DQ}=20mA$ .
100%	Stability into 3:1 VSWR	VSWR-S	--	--	--	$V_{DD}=50V$ , $P_{IN}=10W$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , $F=F1, F2$ , $I_{DQ}=20mA$ . Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
BD	Load Mismatch Tolerance	LMT	--	20:1	--	$V_{DD}=50V$ , $P_{IN}=10W$ , Pulse =50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , $F=F1, F2$ , $I_{DQ}=20mA$ . Rotate 20:1 output VSWR through 360° phase. Survival.
BD	Pulse Risetime	RT	--	60	ms	$V_{DD}=50V$ , $P_{IN}=10W$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , $F=F1, F2$ , $I_{DQ}=20mA$ .
Note 1	F1 =1030 MHz, F2= 1090 MHz.					
Note 2	Pulse format = 50 $\mu$ s, 2%					
Note 3	$T_F$ = Device flange temperature.					
Note 4	Screen 'BD' = parameter qualified By Design.					

**RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

Frequency (MHz)	$Z_{IF}$ ( $\Omega$ )	$Z_{OF}$ ( $\Omega$ )
1030	0.8-j1.43	1.83-j2.21
1090	0.8-j0.91	1.93-j1.7
Impedance Definition		

**PACKAGE DIMENSIONAL OUTLINE DRAWING**

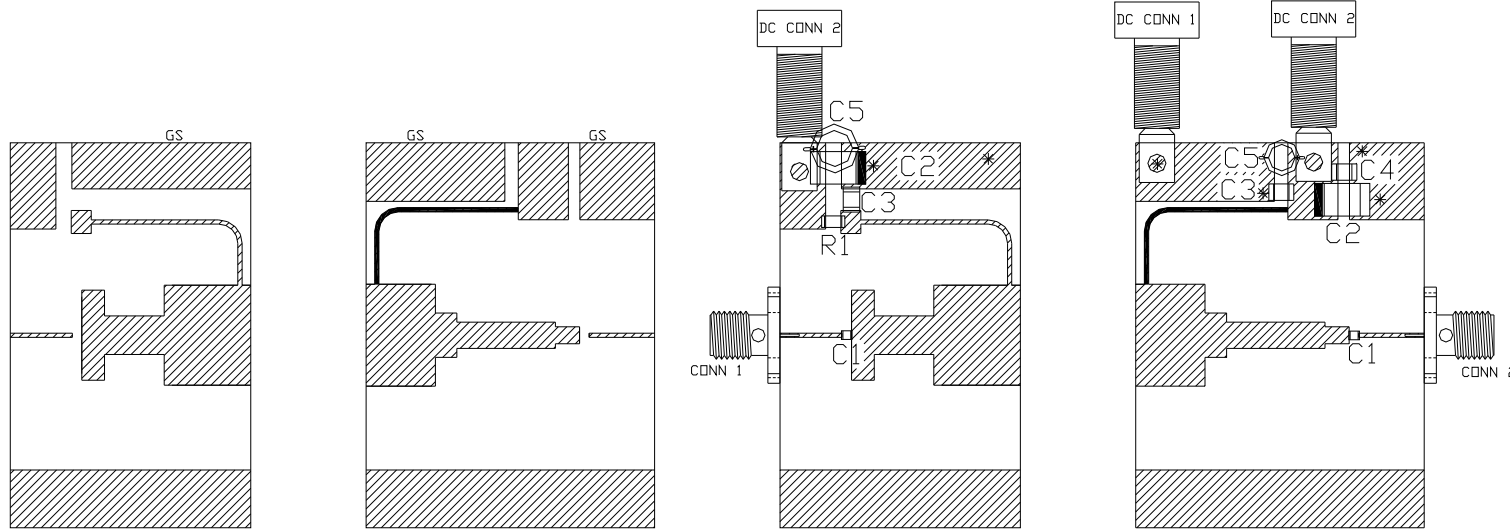


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.535	0.545	13.58	13.84
B	0.035	0.045	0.89	1.14
C	1.335	1.345	33.90	34.16
D	0.147	0.177	3.73	4.50
E	0.123	0.133	3.12	3.37
F	1.095	1.105	27.81	28.06
G	0.035	0.045	0.89	1.14
H	0.170	0.210	4.32	5.33
I	0.170	0.210	4.32	5.33
J	0.003	0.006	0.08	0.15
K	0.495	0.505	12.57	12.82
L	0.364	0.374	9.24	9.49
M	0.772	0.788	19.60	20.01

PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE

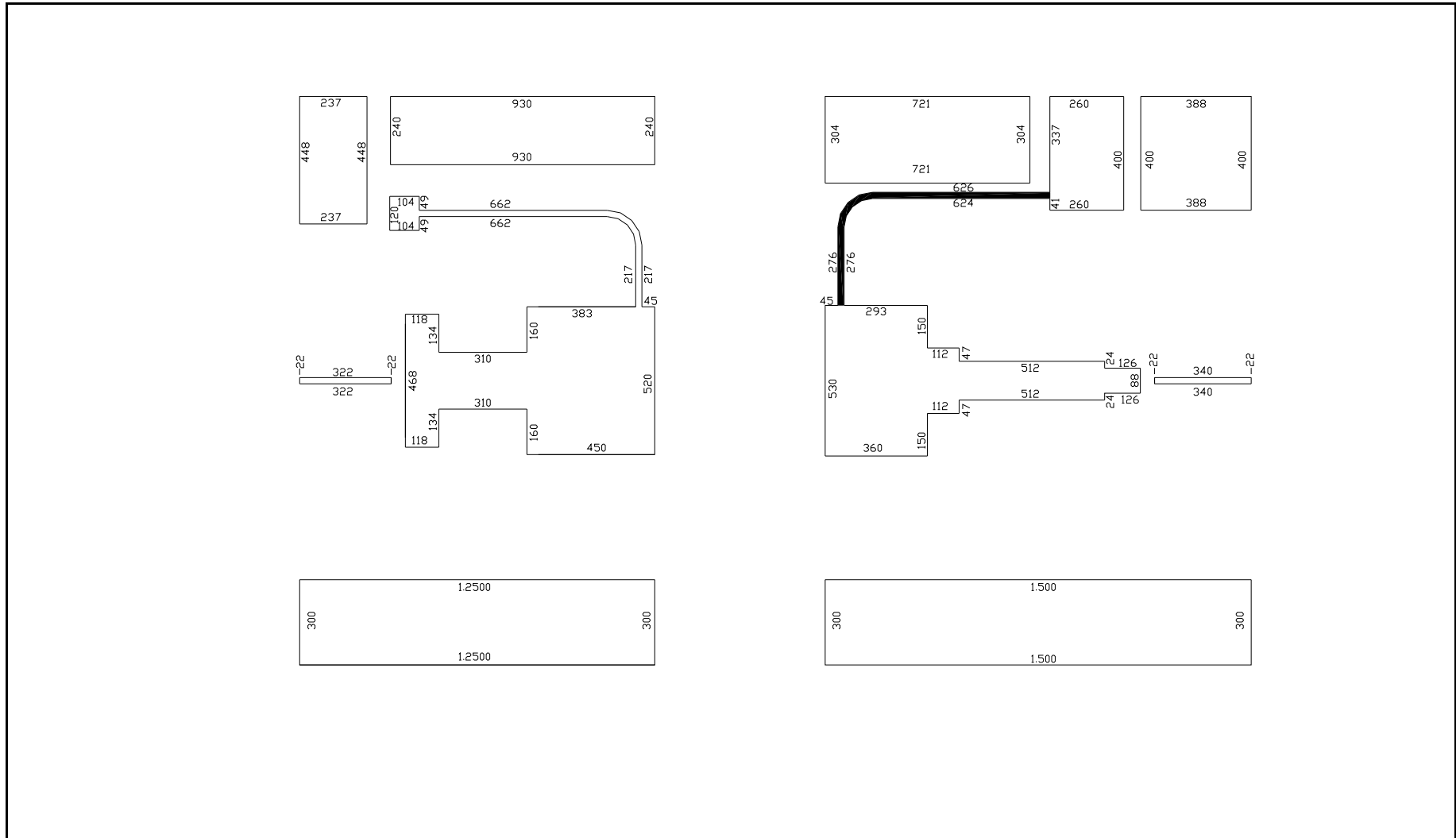
LID-PL84-1

**RF TEST FIXTURE – ASSEMBLY AND PARTS LIST**

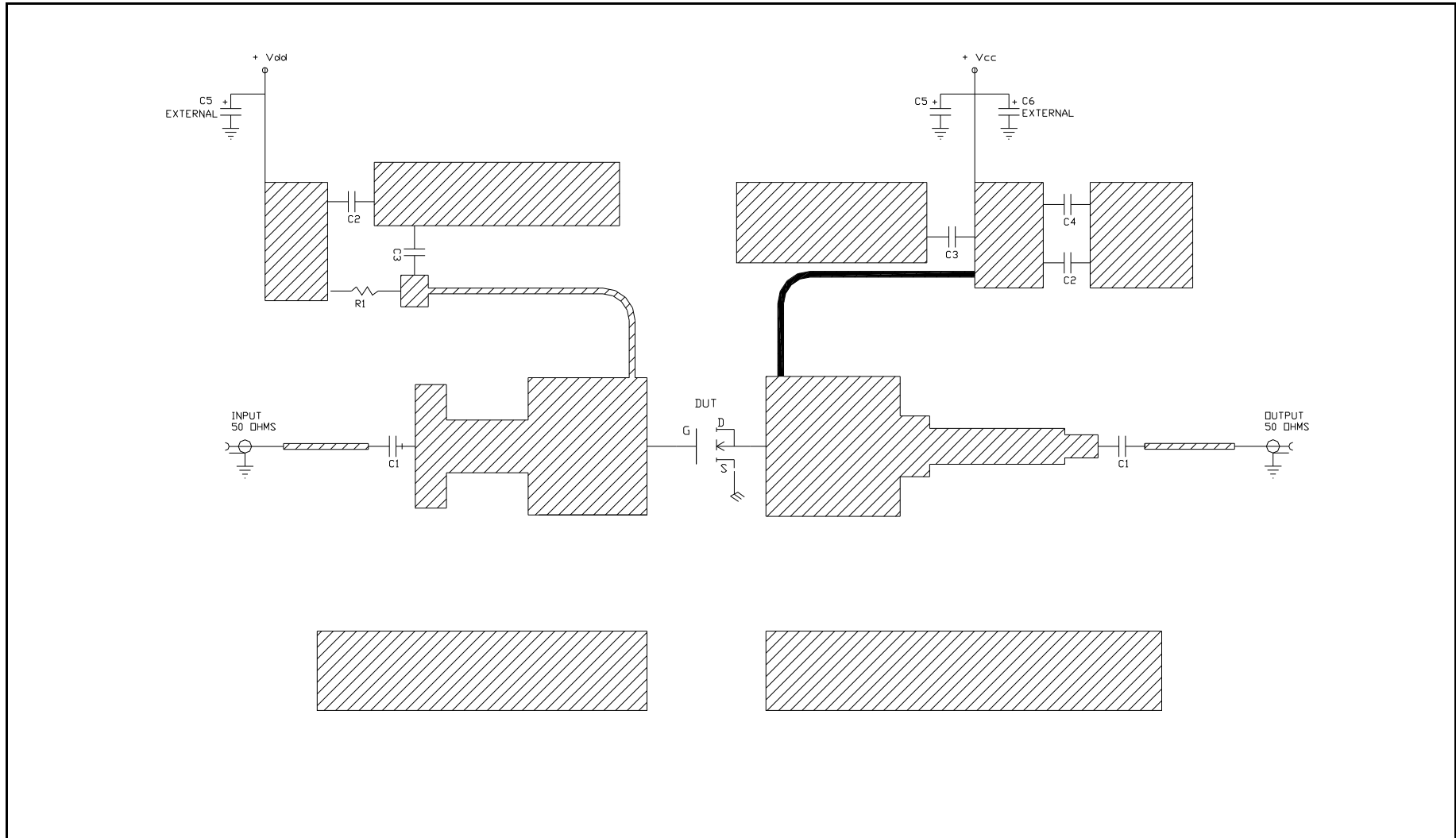


COMPONENT	DESCRIPTION
DUT	TRANSISTOR #IB1011M275HV MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #ROGERS 3010 10.2, .025" 1oz. Cu
C1	CHIP CAPACITOR ATC100A - 39 pF (2 PLCS)
C2	TANTALUM - AVX 4.7uF, 50V ESR = 0.30HMS (2 PLCS)
C3	CHIP CAPACITOR ATC100B - 47 pF (2 PLCS)
C4	CHIP CAPACITOR CERAMIC ATC100B-1000pF 250V (1 PLC)
C5	ELECTROLYTIC CAPACITOR 68uF / 63V
C6 (NOT SHOWN)	ELECTROLYTIC CAPACITOR, 4700uF / 50V
R1	RESISTOR 1206 - 300 OHMS
GS	GROUND SHIM, COPPER, TH=0.001"
CONN 1, CONN 2	SMA CONNECTOR, DS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS-04 (1.25")
OUTPUT PC BOARD CARRIER	2 INCH BRASS-05 (1.5")
TRANSISTOR CARRIER	2 INCH COPPER-22
TRANSISTOR CLAMP	NDRYL CLAMP-07
ALUMINUM HEAT SINK	2 INCH HEATSINK-11
DC CONN 1	BANANA JACK, BLACK
DC CONN 2	BANANA JACK, RED
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST USE CORNELL DUBILIER ALUMINUM FLAT PACK "MLP" SERIES OR SIMILAR FOR STORAGE CAPACITOR.

**RF TEST FIXTURE – CIRCUIT DIMENSIONS IN MILS**



**RF TEST FIXTURE – ELECTRICAL SCHEMATIC**



**DEFINITIONS**

<b>Data Sheet Status</b>	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
<b>Maximum Ratings</b>	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

**DISCLAIMER**

Integra Technologies Inc. reserves the right to make changes without further notice to any products herein. Integra Technologies Inc. makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Integra Technologies Inc. assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Integra Technologies Inc. products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Integra Technologies Inc. customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Integra Technologies Inc. for any damages resulting from such improper use or sale.