

C-Band Radar Transistor - GaN

- GaN on SiC HEMT Technology
- $P_{OUT-PK} = 10W @ 300\mu s/10\%/36V$; ($P_{AVG} = 1W$)
- 5.2-5.9GHz Instantaneous Operating Frequency Range
- Internal Impedance Pre-matched Device
- Depletion Mode Device
- Negative Gate Voltage and Bias Sequencing Required
- Specified For Use Under Class AB Operation
- Metal Based Package Sealed With Ceramic-Epoxy Lid
- Gold Metallization System: Chip - Wire Bond - Package
- Package Size: W=0.800" (20.32mm), L=0.230" (5.84mm)
- 100% High Power RF Tested in Broadband RF Test Fixture

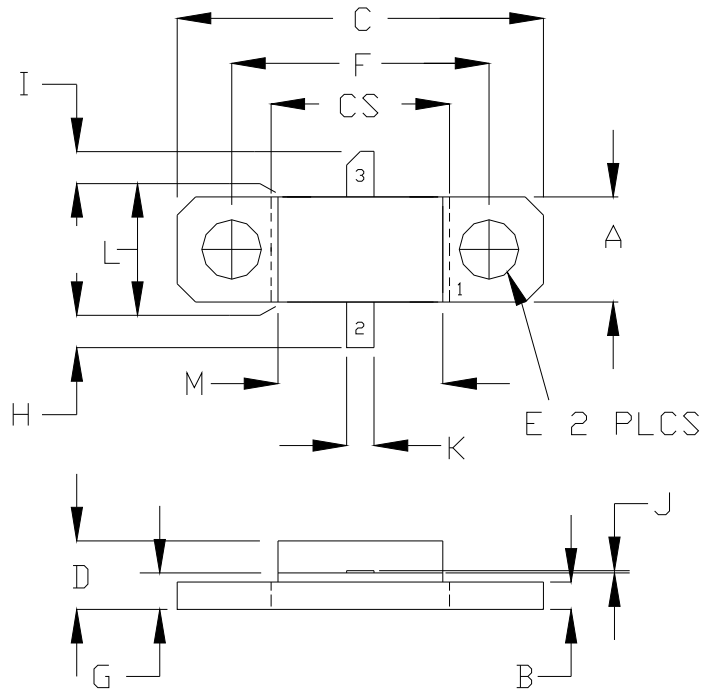


| PARAMETER | SYM | MIN | TYP | MAX | UNITS | TEST CONDITIONS |
|-------------------------------------|-------------|-------|-------|-------|-------|---|
| DC ELECTRICAL SPECIFICATIONS | | | | | | |
| Drain Leakage Current | I_{D-OFF} | -- | 0.5 | 1.0 | mA | $V_{DS}=36V, V_{GS}=-6V, T_{F1}, S1$ |
| Gate Threshold Voltage | V_{GS-TH} | -- | -4.0 | -- | V | $V_{DS}=5V, I_D=10mA, T_{F1}, BD$ |
| RF ELECTRICAL SPECIFICATIONS | | | | | | |
| Input Return Loss | IRL | -18 | -12 | -7 | dB | POUT1, V1, I_{DQ1} , PW1, DF1, F1, F2, F3, $T_{F1}, S1$ |
| Power Input | PIN | 0.32 | 0.50 | 0.80 | W | POUT1, V1, I_{DQ1} , PW1, DF1, F1, F2, F3, $T_{F1}, S1$ |
| Power Gain | G_p | 10.97 | 12.50 | 14.95 | dB | POUT1, V1, I_{DQ1} , PW1, DF1, F1, F2, F3, $T_{F1}, S1$ |
| Drain Efficiency | η_D | 48 | 55 | 75 | % | POUT1, V1, I_{DQ1} , PW1, DF1, F1, F2, F3, $T_{F1}, S1$ |
| Pulse Amplitude Droop | D | -0.50 | -0.10 | +0.30 | dB | POUT1, V1, I_{DQ1} , PW1, DF1, F1, F2, F3, $T_{F1}, S1$ |
| Delta Inter-pulse Insertion Phase | DIP | -30 | -- | +30 | DEG | POUT1, V1, I_{DQ1} , PW1, DF1, F3, $T_{F1}, S1$ |
| Load Mismatch Stability | VSWR-S | 3:1 | -- | -- | -- | POUT1, V1, I_{DQ1} , PW1, DF1, F1, F2, F3, $T_{F1}, S1$ |
| DC & RF TEST CONDITIONS | | | | | | |
| Output Power 1 | POUT1 | -- | 10 | -- | W | -- |
| Drain Supply Voltage 1 | V1 | -- | -- | 36.0 | V | -- |
| Quiescent Drain Current 1 | I_{DQ1} | -- | -- | 10 | mA | -- |
| Pulse Width 1 | PW1 | -- | -- | 300 | us | -- |
| Duty Factor 1 | DF1 | -- | -- | 10 | % | -- |
| Frequency 1 | F1 | -- | 5.20 | -- | GHz | -- |
| Frequency 2 | F2 | -- | 5.55 | -- | GHz | -- |
| Frequency 3 | F3 | -- | 5.90 | -- | GHz | -- |
| Flange Temperature 1 | T_{F1} | 25 | 30 | 35 | °C | -- |
| Screening Level 1 | S1 | 100 | -- | -- | % | -- |

| PARAMETER | SYM | MIN | MAX | UNITS | SCREEN | CONDITIONS |
|--|--------------|-----|------|--------------------|--------|--------------------------|
| MAXIMUM RATINGS | | | | | | |
| Drain-Source Voltage | V_{DS} | -- | 36 | V | BD | $T_F = 25^\circ\text{C}$ |
| Gate-Source Voltage | V_{GS} | -10 | 0 | V | BD | $T_F = 25^\circ\text{C}$ |
| Storage Temperature Range | T_{STG} | -55 | +150 | $^\circ\text{C}$ | BD | -- |
| Operating Junction Temperature | T_J | -55 | +200 | $^\circ\text{C}$ | BD | -- |
| PROCESS SPECIFICATIONS | | | | | | |
| DC Wafer Probe | -- | -- | -- | -- | 100% | Per Integra Spec |
| Wafer DC, RF Qualification | -- | -- | -- | -- | Q1 | Per Integra Spec |
| Wire Bond Strength | -- | -- | -- | -- | LM | Per Integra Spec |
| Pre-cap Visual Inspection | -- | -- | -- | -- | 100% | Per Integra Spec |
| Gross Leak Test – MIL-STD-750D | -- | -- | -- | -- | 100% | Method 1071.6 C |
| THERMAL RESISTANCE | | | | | | |
| Peak Thermal Resistance Per Rated RF Specification | $R_{TH(JC)}$ | -- | 2.25 | $^\circ\text{C/W}$ | BD | $T_F = 25^\circ\text{C}$ |
| SCREENING LEVELS | | | | | | |
| Parameter Qualified By Design | BD | -- | -- | -- | -- | -- |
| Parameter Qualified By 3 Pieces (min) Per Wafer | Q1 | -- | -- | -- | -- | -- |
| Parameter Qualified By Assembly Line Monitor | LM | -- | -- | -- | -- | -- |

| RF TEST FIXTURE – BROADBAND | | |
|--|------------------|------------------|
| ▶ Broadband RF Test Fixture. Provides Device Impedance Matching to 50Ω Across the Rated Operating Frequency Range. | | |
| ▶ Electronic CAD Drawing File Available Upon Request. Includes Circuit Dimensions and Parts List. | | |
| ▶ Reference Design PCB: Rogers RO4350B-03011, DK=3.48. | | |
| FREQUENCY (GHz) | $Z_{IF}(\Omega)$ | $Z_{OF}(\Omega)$ |
| 5.20 | 7.7 – j18.1 | 12.5 – j4.8 |
| 5.55 | 9.6 – 16.3 | 13.4 – j0.6 |
| 5.90 | 8.8 + j14.2 | 12.3 + j4.0 |
| Impedance Definition | | |

PACKAGE OUTLINE DRAWING



'S' VERSION USE DIM CS
NON 'S' VERSION USE DIM C

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.225 | 0.235 | 5.71 | 5.96 |
| B | 0.055 | 0.065 | 1.40 | 1.65 |
| C | 0.795 | 0.805 | 20.19 | 20.44 |
| CS | 0.385 | 0.395 | 9.78 | 10.03 |
| D | 0.140 | 0.160 | 3.55 | 4.06 |
| E | 0.125 | 0.135 | 3.18 | 3.43 |
| F | 0.557 | 0.567 | 14.14 | 14.40 |
| G | 0.077 | 0.087 | 1.95 | 2.20 |
| H | 0.093 | 0.107 | 2.36 | 2.72 |
| I | 0.093 | 0.107 | 2.36 | 2.72 |
| J | 0.004 | 0.006 | 0.10 | 0.15 |
| K | 0.055 | 0.065 | 1.40 | 1.65 |
| L | 0.225 | 0.235 | 5.71 | 5.96 |
| M | 0.355 | 0.365 | 9.01 | 9.27 |

| PIN SCHEDULE | |
|--------------|--------|
| 1 | SOURCE |
| 2 | GATE |
| 3 | DRAIN |

NOTE: LID-PL32-1

| DEFINITIONS | |
|--|---|
| DATA SHEET STATUS | |
| Proposed Specification | This data sheet contains proposed specifications. |
| Preliminary Specification | This data sheet contains specifications based on preliminary measurements and data. |
| Product Specification | This data sheet contains final product specifications. |
| MAXIMUM RATINGS | |
| Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability. | |

| DISCLAIMER |
|--|
| Integra Technologies Inc. makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Integra Technologies Inc. assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Integra Technologies Inc. products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Integra Technologies Inc. customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Integra Technologies Inc. for any damages resulting from such improper use or sale. |