

Handling and Adjustment of Integra Technologies Bipolar Transistor Evaluation Kits

INTRODUCTION

Integra Technologies loans evaluation kits to customers. Evaluation kits consist of a test fixture with one transistor already mounted inside it together with our test results, plus a spare transistor. For our Si bipolar devices then the evaluation kit will be for an IBxxxx part which is a transistor that may or may not be partially matched within the transistor package to 50Ω . All of our bipolar transistors incorporate emitter ballast resistors in order to prevent thermal runaway.

Si BIPOLAR TRANSISTOR BIASING

Our Si bipolar transistors are NPN devices that are configured within the package to operate in a Common Base mode. Thus the input terminal of the package is connected to the emitter, the output lead is connected to the collector, and the base is connected to the package flange. The input terminal of the package (i.e. the emitter) is connected to ground at DC in the test fixture and so no external bias to the base-emitter junction is either required or is possible. Only a single power supply is required to provide a positive voltage to the V_{CC} terminal

on the test fixture.

In the absence of any applied RF signal then no base current is injected into the collector and so, in the ideal case, no collector current will flow when a positive voltage is applied to the collector. Note that application of a positive voltage to the collector reverse biases the collector-base junction and so the only current that flows when there is no applied RF voltage is the finite reverse-biased collector-base junction diode leakage current. The maximum value for this current is specified in the data sheet by the parameter I_{CES} which is typically $<1\text{mA}$. The user should check that the collector current is $<I_{CES}$ when the correct voltage is applied to the V_{CC} terminal before applying any RF signal. It should also be noted that the absence of any collector current (apart from the very small leakage current I_{CES}) in the RF-off period of a pulsed signal is particularly beneficial in radar systems as it results in negligible injection of shot noise into the receiver in the off-period which would otherwise cause receiver desensitization. This is an important advantage of bipolar transistors compared with LDMOS and GaN HEMT devices that are always biased in Class A/B.

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When an RF signal is applied at the input then no emitter-base current will flow until the magnitude of the RF input voltage exceeds the turn-on voltage of the emitter-base junction which is typically around 0.7V. The transistor is thus operating in Class C mode which results in a non-linear P_{in} versus P_{out} curve. This situation is further exacerbated by the fact that the emitter-base current, and hence the collector current, has an exponential dependence on the applied base-emitter voltage. Consequently, bipolar transistors exhibit substantial gain expansion before the onset of gain compression. This phenomenon is inherent in Class C operation of Si bipolar RF transistors and is fundamentally different to the usual almost-constant gain followed by gain compression characteristic exhibited by LDMOS transistors. However, a by-product of Class C operation of bipolar transistors is that they have higher efficiency than a comparable LDMOS transistor. Figure 1 shows a graph of gain versus P_{out} for Integra's Si bipolar transistor IB0912M500 under Mode S operation at 1090MHz. The gain curve clearly shows the typical gain expansion followed by gain compression characteristic as well as the high efficiency of almost 70% - around 15 percentage points higher than for a comparable LDMOS transistor. Note that peak efficiency and peak gain occur at almost the same output power.

Finally, while in theory Class C operation results in a significant harmonic content in the output current (and it is essential that the harmonics are allowed to flow in order to get high efficiency), these harmonic current components are short-circuited to ground within the transistor package by the transistor's own internal collector-base capacitance and by the capacitors used in

the internal matching at the output of the transistor so that harmonic levels are subdued at the output of the transistor.

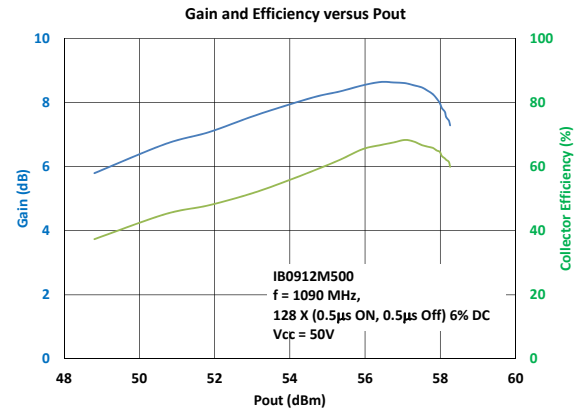


FIGURE 1: Typical gain and efficiency of a Class C Si bipolar transistor as a function of output power.

The following sequence should be followed when testing the transistor:

1. Make sure that the RF is turned off before installing the test fixture in the test bench. Make sure that the proper pulse width and duty cycle have been properly set on the RF source prior to turning on the transistor. The transistor may be damaged if the RF source is not set for the correct pulse format.
2. Ensure that the test bench presents good 50 ohm source and load impedances to the evaluation kit with, ideally, around 30dB return loss. The output must have a load capable of handling ~3dB more power than both the rated peak output power and the average output power of the transistor.
3. Check the screw torque on the transistor clamp to ensure that the clamp has not loosened during shipment. The screws should be torqued sequentially to between 6-8 in/lbs.
4. Connect the charge storage capacitor across the V_{CC}

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(RED) and GND (BLACK) terminals. This capacitor usually has a value of 4700 μ F. This capacitor is needed to minimize pulse droop when the RF signal is applied. After first ensuring that the power supply is switched off, connect the power supply to the test fixture with the positive output connected to the RED terminal (V_{CC}) and the GND connected to the BLACK terminal.

- Next set the power supply current limit such that it, in conjunction with the charge storage capacitor, it can handle the maximum peak current expected for the device. Next attach the power supply's voltage sense leads to the V_{CC} and $V_{CC, GND}$ terminals if the power supply has this feature available. Ensure that the power supply is in its remote current sense mode. If the power supply does not have a voltage sense capability then connector a voltmeter across the RED and BLACK terminals on the test fixture and manually adjust the collector voltage during RF testing to compensate for any voltage drop.
- Turn on the collector bias voltage and slowly increase it until the voltage reaches the specified value for V_{CC} in the data sheet. Ensure that the collector current does not exceed the value given by I_{CES} in the data sheet.
- Turn on the RF input power starting at a low power (< 0.1W peak), and then increase until the desired output power is achieved. Correlation data is supplied with the clamped device. Please verify correlation with Integra's test results before changing the transistor. The detected RF output pulse should be monitored to ensure that no break up occurs as this may indicate the presence of an oscillation. Ensure that the RF input power never exceeds the maximum permitted value specified on the data sheet as bipolar transistors are much less forgiving on surviving an overdrive than LDMOS. This follows as

a consequence of the efficiency decreasing as the output power increases beyond the optimum value shown in Figure 1 leading to a rapid rise in junction temperature under overdrive.

- After the testing is complete turn off the $+V_{CC}$ collector supply voltage first but leave the RF applied for about 5 seconds to discharge the large collector charge storage capacitor. Next, turn off the RF power.

DEVICE CORRELATION

The evaluation kit includes the test fixture, an electrolytic capacitor, two transistors, and our RF test data. One of the devices is already clamped into the test fixture. The device has been tested at Integra as installed, and should be used for correlation purposes. Please compare your measured data with Integra's RF data for the serial number installed in the test fixture and reconcile any discrepancies before removing or changing the transistor.

EFFICIENCY MEASUREMENT

Please note that the efficiency recorded in our test data is collector efficiency and not power-added efficiency.

TEMPERATURE COMPENSATION

The test fixture does not incorporate any temperature compensation.

COOLING

The transistor will dissipate power and requires adequate cooling. As a minimum a biscuit-fan model BT2A1 or

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equivalent should be provided. This fan can provide 22CFM of airflow over the fins of the heat sink. A #4-40 UNC threaded screw hole is located on the copper carrier underneath the transistor to monitor the flange temperature. The typical flange temperature for RF testing is $30^{\circ}\text{C}\pm 5^{\circ}\text{C}$.

CHANGING THE TRANSISTOR

1. Thermal grease was used for testing this part. Assuming that the heatsink of the test fixture has been cleaned, then only a small dot of grease 0.03-0.04" in diameter should be applied in the center of the slot. Do not use an excessive amount of grease. The grease pattern after transistor removal should not extend by more than 0.25". The correct amount of grease is required to obtain a thin coat that will not degrade electrical contact. Use Wakefield 120 [1] or equivalent thermal grease.
2. Make sure that the clamp is properly seated on the top of the flange, and that the screws are torqued sequentially to between 6-8 in/lbs.

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between the leads and the metal flange is a beryllium oxide substrate. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area which might create any beryllium oxide dust.

THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE AND MUST BE DISPOSED OF IN AN APPROVED MANNER.

CONCLUSION

This Application Note has described how to safely use and adjust Integra's bipolar evaluation Kits. If additional information is required then please contact Integra Technologies.

REFERENCES

1. <http://www.wakefield-vette.com/resource-center/downloads/brochures/thermal-management-accessories-wakefield.pdf>