INTEGRA
RF POWER DEVICES

Handling and Adjustment of Integra Technologies GaN-on-SiC Pallets

INTRODUCTION

Integra Technologies manufactures a range of GaN on SiC HEMT pallets. These can be categorised by the number of transistors that they incorporate (one or two) and by whether or not they incorporate **G**ate **P**ulsing and **S**equencing (**GPS**) circuitry. If the pallet contains a single transistor then the pallet will incorporate RF matching circuitry so that it can operate directly in a 50 Ohm system. This means that the input reflection coefficient S_{11} is close to zero, but in the case of the output it means that the correct load that needs to be attached to the pallet is 50 Ohms, it does not mean that S_{22} is close to zero, in fact its magnitude is likely to be close to unity. If the pallet contains two transistors then these will be combined in-phase using either a Wilkinson [1] or Gysel [2] combiner/divider network. The output power of the pallet will then be twice that of an individual transistor. The pallet will present an excellent VSWR at the input but it will still present an output VSWR close to being totally reflecting..

If the pallet incorporates GPS circuitry then the pallet only requires a single positive supply voltage, all other voltages are generated within the pallet. GPS provides an automtatic and fail-safe biasing system that prevents accidental damage to the pallet as a result of not applying the gate and drain voltages in the correct sequence. The operation of the GPS system is described in detail in Integra Technologies Application Note 004 which is available for download from the Integra web site www.integratech.com.

PALLET BIASING AND TURN-ON SEQUENCE FOR PALLETS WITHOUT GPS

GaN HEMT devices are depletion mode transistors and so extreme care is needed to ensure that the correct biasing sequence is followed or else the transistor(s) in the pallet is (are) likely to be destroyed. The transistor requires that a negative voltage be applied to the gate and that this must be applied before any positive voltage is applied to the drain. Thus at least two separate power supplies are required, one or two to supply a negative voltage to the gate(s) and one to supply a positive voltage to the drain. In the case of a pallet with two transistors then both devices should use the same drain power supply even though the pallet is likely to have two separate drain terminals. This issue is discussed further

later on.

The following sequence should be followed when testing the pallet:

1.. Ensure that the test bench presents good 50Ω source and load impedances to the pallet with, ideally, around 30dB return loss. The output must have a load capable of handling ~3dB more power than both the rated peak output power and the average output power of the pallet.
2. After first ensuring that it is fully discharged, attach a large value electrolytic capacitor e.g. 4700μF between the drain terminal(s) and ground. This capacitor should be placed as close as possible to the drain terminal. This capacitor is needed to minimise pulse droop, especially for long pulses.
3. The gate bias supply voltage should be adjustable over a range of at least -5V to -2V. The positive terminal of the gate supply voltage must be connected to the pallet ground, and the negative terminal connected to the gate bias pad or socket on the pallet. **Applying a positive voltage to the gate will destroy the transistor!** Set the current limit on the gate supply to 100mA maximum. The gate supply must be able to source and sink current. At low RF power, the negative supply applied to the gate will sink a current of a few mA due to the finite leakage current of the transistor. However, at high RF input power rectification of the RF input signal will occur due to the Schottky gate within the transistor. This causes the direction of the gate current to reverse and so now the gate supply must source current. Most bench power supplies cannot source and sink current. This problem can be solved by connecting a shunt resistor across the terminals of the gate power supply as shown in Figure 1.

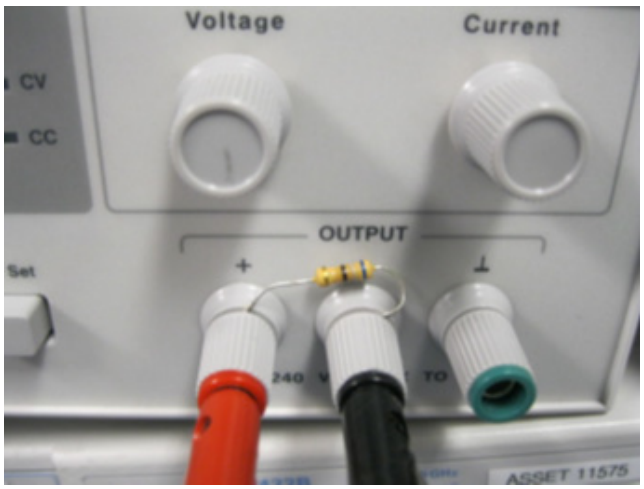

FIGURE 1: Configuring the gate power supply to both sink and source gate current.

The value of R_{shunt} is determined by:

$$R_{shunt} < \frac{V_{GS,max}}{I_{GS,max}} \quad (1)$$

For $V_{GS,max}$ = 4.5V and $I_{GS,max}$ = 10mA, then R_{shunt} < 450Ω. In Figure 1 a value of 67Ω was used. The resistor power rating should be > $V_{GS,max}$ x $I_{GS,max}$ i.e. >45mW in this example.

4. Set the gate supply voltage to -5V to each transistor. Verify that the voltage on each transistor gate is -5V relative to the heat sink. Measure the resistance between the drain(s) and the ground terminal. You should measure around 10kΩ through the device drain if the gate supply voltage is properly applied since the channel is turned off.
5. After first ensuring that the drain power supply is switched off, connect the drain power supply to the pallet with the positive output connected to the drain terminal and the ground connected to the pallet

baseplate. If the pallet has two transistors then both drain terminals should be connected to the same power supply. This not only makes it easy to measure the total pallet current consumption and hence to determine its efficiency and is the way that pallets are tested at Integra, it also ensures that while the quiescent current is being set on the first transistor that the other one presents a similar impedance to the combiner. The output impedance of the transistor is strongly dependent on whether or not the drain has a voltage applied to it, and without a drain voltage there is the possibility of instability occuring while setting the quiescent current of the first side. Set the power supply current limit such that, in conjunction with the charge storage capacitor, it can handle the maximum peak current expected for the pallet.

6. Turn on the drain power supply and set V_{DD} to the value specified in the data sheet for the pallet. There should be less than 10mA of current drawn by the pallet from the drain power supply since the gate bias to the transistor(s) is at -5V to keep the device in pinch off.
7. SLOWLY increase the gate voltage (make less negative) to one of the transistors from -5V until the quiescent current I_{DQ} specified in the pallet's data sheet is achieved. If the pallet incorporates two transistors, then the data sheet will specify the total quiescent current when both transistors are operating so each transistor needs a quiescent current of half that of the complete pallet. The gate voltage increment should not exceed 50mV to prevent overdriving the gate voltage, thereby inducing excessive drain current and potentially burning out the device. An Agilent E3610A power supply or equivalent is suitable. The gate voltage will typically be around V_{GS} = -2.7V to achieve the recommended I_{DQ} value. A spectrum analyzer should be connected at the output to ensure that no oscillations occur as the gate voltage is increased since oscillations can sometimes result in device destruction.

   If the pallet contains two transistors then repeat the above procedure for the second transistor while the first one is still operating until the drain current now equals the total pallet quiescent current specified in the data sheet.
8. Turn on the RF input power starting at a low power (< 0.1W peak), and then increase until the desired output power is achieved. Integra's measured data is supplied with the pallet. Please verify correlation with Integra's test results. The detected RF output pulse should be monitored to ensure that no break up occurs as this may indicate the presence of an oscillation.
9. After the testing is complete turn off the $+V_{DD}$ drain supply voltage first but leave the RF applied for about 5 seconds to discharge the large drain charge storage capacitor. Next, turn off the RF power. Lastly, turn off the gate supply voltage.

EFFICIENCY MEASUREMENT

Please note that the efficiency recorded in our test data is drain efficiency and is not power-added efficiency. Integra calculates the efficiency from the product of the drain voltage and the average current drawn from the supply divided by the duty cycle. However, the transistor is drawing its quiescent current from the power supply when there is no RF signal applied and this effect is not allowed for in our efficiency data. Consequently, our drain efficiency data underestimates the true efficiency.

REFERENCES

1. E.J. Wilkinson, "An N-Way Hybrid Power Divider", IRE Trans. microwave Theory and Techniques, Vol. MTT-8, pp. 116-118, Jan 1960.

2. U. H. Gysel, "A New N-Way Power Divider/Combiner Suitable for High-Power Applications", IEEE MTT-S International Symposium Digest, pp. 116-118, 1975