INTEGRA
RF POWER DEVICES

Effect of Tolerances on Microstrip Impedance and Power Output

INTRODUCTION

An often-asked question is why does my amplifier performance vary from unit to unit, or why does my amplifier performance differ from that predicted by the model? This application note addresses primarily the former issue but will first very briefly discuss the first.

As far as measured performance that differs from that predicted by the model is concerned, then there are both systemic as well as random effects. Any circuit design that uses a model for the transistor assumes that every transistor manufactured has the exact same performance as that of the model, but this is of course manifestly untrue. The transistor model is based on an 'average' transistor across a large number of devices and so there will always be a random variation in performance across a number of amplifiers compared to that predicted by the model just due to that effect alone. There are also random variations introduced simply because the components such as capacitors have an associated tolerance that ranges from ±1% to ±20% for a 33pF ATC600F330 capacitor depending on the grade of capacitor chosen. Finally, there are systemic variations between the simulated and measured performance that arise because the amplifier realization is not an exact implementation of the circuit design, but these effects are constant across all manufactured amplifiers, for example the passband of the amplifier might be 100MHz lower across all samples than predicted. There are techniques for minimizing this effect, but these are beyond the scope of this particular Application Note.

Engineers are familiar with how to take account of capacitance variations, for example, because the parameter that is varying is capacitance and so its effect is readily determined by a simulator such as Microwave Office. In some cases a simple arithmetic calculation is all that is needed e.g. to determine the resonant frequency of an LC circuit. However, in the case of printed circuits manufactured using a substate then the parameters that are varying are mechanical (thickness of the substrate and the metalization, width of the etched microstrip line) and material (dielectric constant) and not electrical directly such as impedance or electrical length. Thus, variations in these parameters on electrical performance are harder to quantify. This Application Note shows the effect of these variations on impedance and electrical length for one particular substrate, namely 25 mil thick RT Duroid RO6010.2LM with 1oz copper. The resulting change in impedance and electrical length can be readily

determined using any standard circuit simulator such as Microwave Office or ADS. However, for this Application Note a simpler approach was adopted using an on-line calculator [1]. Strictly speaking, metalization thickness probably shouldn't be listed as a tolerance as the user has to specify what thickness they require when the order for the substrate is placed. The thickness is specified via the weight of copper deposited, and this weight has maximum and minimum limits of 0.5 to 2 oz/ft^2 which translates into a thickness of 18 to 70μm. For this study a nominal 1 oz/ft^2 was chosen as the baseline.

Table 1 lists the tolerances given by the manufacturer for RO6010.2LM substrates. Relative to its nominal value, both parameters in Table 1 have a 6% tolerance.

Parameter	Nominal Value	Tolerance
Dielectric constant	10.2	+/- 0.25
Thickness	0.025"	+/- 0.0015"

TABLE 1: Tolerances for RO6010.2LM substrates as specified by the manufacturer

Table 2 lists the effect of these individual tolerances on the characteristic impedance of a 50 Ω line when fabricated on a substrate having its nominal values for dielectric constant and thickness.

Parameter	Minimum Value of Z_0 Ω	Maximum Value of Z_0 Ω
Dielectric constant	49.4	50.6
Dielectric Thickness	48.5	51.4
Metallization Thickness	49.1	50.6

TABLE 2: Effect of tolerances on the characteristic impedance of a microstrip line

It can be seen from Table 2 that the characteristic impedance has the same sensitivity to metallization thickness as it does to dielectric constant, but the tolerance on dielectric thickness has the greatest effect. The capacitance to ground, which determines the characteristic impedance, has an inverse dependence on substrate thickness while it has an approximate square root dependence on dielectric constant which explains why the characteristic impedance is more sensitive to substrate thickness than to dielectric constant variations.

Taking the highest value for dielectric constant and metallization thickness and the lowest value for dielectric thickness, and vice versa, will give the worst-case scenario which is given in Table 3. It be seen that the characteristic impedance has an overall tolerance of ±1% due to the tolerances associated with the substrate.

Lowest Value for Z_0 Ω	Highest Value for Z_0 Ω
49.4	50.6

TABLE 3: Worst case values for characteristic impedance of a microstrip line due to tolerances

width will also vary from its intended value. For isotropic etches then the metal is etched both laterally and vertically to the same extent which results in the metal exhibiting undercut at the edge. Thus for 1 oz Copper which has a thickness of 36 μm then the metal will show an undercut on both edges of 36μm with an isotropic etch. This undercut will result in the line having a higher impedance than its intended value, but this effect can be allowed for in the design by deliberately making the line wider than would be required if undercut didn't exist. The

undercut is independent of line width and so the characteristic impedance of narrow high-impedance lines is affected more than for a wide low-impedance line. Table 4 quantifies this effect for three different microstrip lines with 36μm metal thickness and linewidth reduced by 36μm on both sides (for simplicity the line profile is assumed to still be rectangular rather than trapezoidal).

Parameter	Z_0 Ω	Z_0 Ω	Z_0 Ω
Characteristic impedance without undercut	25	50	80
Characteristic impedance without undercut	25.6	53	93.4

TABLE 4: Effect of undercut on the characteristic impedance of a microstrip line

While line width tolerance might appear to be a major issue, fortunately the basic physics of a microwave transistor amplifier work in our favor to mitigate this effect. A typical high power microwave transistor amplifier requires that the transistor see a resistive load in the low Ohm to sub-Ohm range and this is generally achieved by using one or more low impedance quarter-wave transmission lines which, as the table shows, are much less sensitive to line width tolerance. The bias is often fed to the transistor drain or collector via a high impedance quarter-wave transmission line which is shorted at the far end via a high value capacitor. The higher the impedance of this bias line the better so undercut here is an advantage.

The above has considered the effect of tolerances on just the characteristic impedance, but they also affect the electrical length of a transmission line. Performing a similar analysis to that above then the worst-case tolerance on electrical length at 1 GHz is ±2.5%.

Finally, of crucial importance is the tolerance associated with assembly. The amplifier is typically constructed with either a hole milled out in the PCB or else it uses a separate substrate for input and output matching networks. In either case, the distance between the input and output matching networks is of necessity slightly larger than the flange width of the transistor. Consequently, the amplifier can be assembled with the transistor centered in the gap or hole, or pushed closest to either the input or output network. It should always be pushed closest to the output network as even a small gap creates a series inductance. At 3 GHz even 0.1nH has a reactance of nearly 2 Ω which is of the same order of magnitude as the optimum load impedance that the transistor needs to see and so the gap detunes the output and results in a loss of output power. Another critical assembly-related issue is getting the leads of the transistor to be exactly coplanar with the PCB and to lie directly on top of it when the transistor is inserted. If the leads are above the PCB and pushed down during the solder process then this also creates a series inductance.

This Application Note will now consider two practical examples of the effect of tolerances on amplifier performance. The first is a Silicon bipolar transistor amplifier based on Integra's IB2729M170 which is a 170W transistor for S band radar applications while the second is a GaN on SiC HEMT amplifier based on IGN2731M180. For the bipolar device the effects of tolerances were first determined via simulation of the PCB layout and then verified by electrical measurements, while for the GaN device the effects of tolerances were determined via a non-linear model for the transistor.

IB2729M170

Figure 1 shows the test fixture layout for this transistor while Figure 2 shows just the PCB layout for the input and output matching networks.

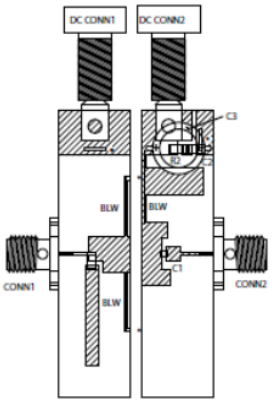

FIGURE 1: IB2729M170 test fixture

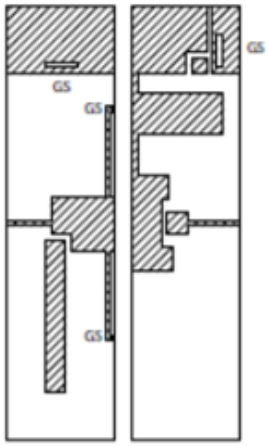

FIGURE 2: IB2729M170 Input and output matching network PCB layout

Both the input and output matching networks were simulated in Microwave Office to determine the impedance presented to the input and output of the transistor, and then the nominal values of dielectric constant, dielectric thickness and line width were varied using the max/min values for these parameters as given previously to determine the spread in the impedances that could be presented to the transistor. The result of this is given in Figures 3-5 where only one parameter is varied at a time for a single frequency, namely 2.9 GHz, while Figure 6 shows the worst-case scenario where all parameters are varied simultaneously.

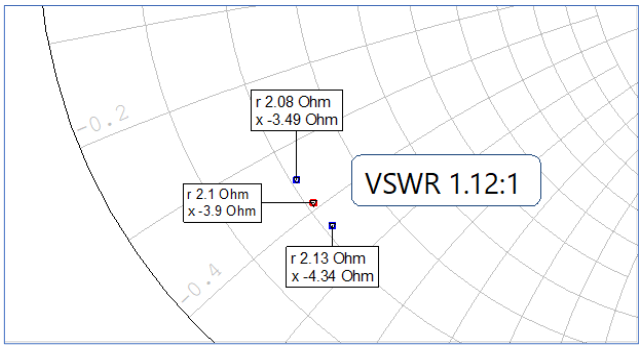

FIGURE 3: Effect of varying the line width by +/- 2 mils with substrate thickness = 25 mils and ε_r = 10.2.

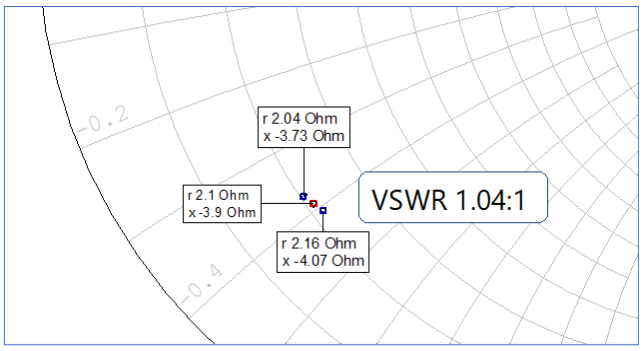

FIGURE 4: Effect of varying the substrate thickness by +/- 1.5 mils with nominal line widths and ε_r = 10.2

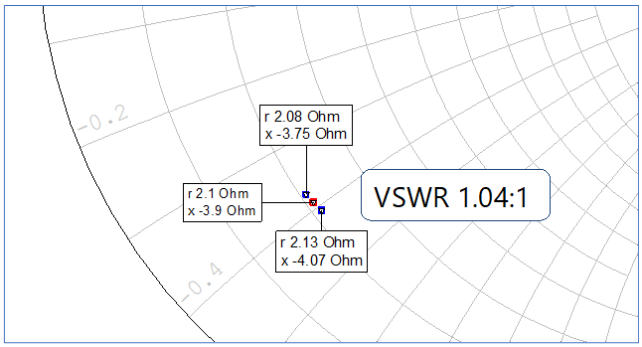

FIGURE 5: Effect of varying ε_r by +/- 0.25 with nominal line widths and substrate thickness = 25 mils.

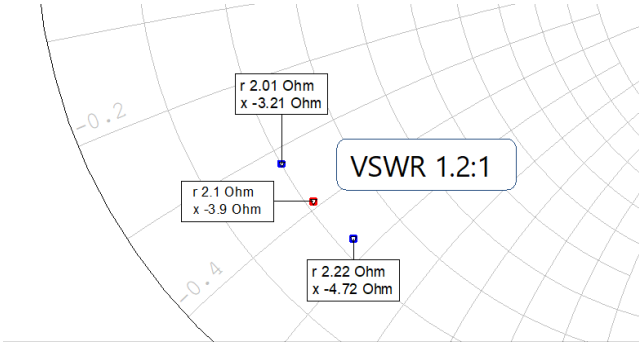

FIGURE 6: Worst-case scenario when all tolerances add up.

It can be seen that the real part of the load impedance hardly varies, it is almost within measurement error, but the imaginary part varies considerably, and certainly greater than measurement error. Note also that 0.1 nH inductance, which is equivalent to 2 Ω at 2.9 GHz at the output of the transistor, caused by positional variations in mounting, will have a far more significant de-tuning effect than any effect of substrate variations.

In order to determine the effect of these impedance variations on the RF output power it was necessary to investigate this effect experimentally since a non-linear model isn't available for this transistor. A representative example of IB2729M170 was first tested in our standard production test fixture in which it delivered 175W with 8.1 dB gain at 2.9 GHz. Then a 1.2:1 VSWR mismatch was inserted externally to the test fixture and its phase varied over the full 360^0., and the worst- and best-case power and gain was recorded. This showed that the power and gain varied between 163 and 180 W and 7.8 and 8.3 dB, respectively. However, any variation in dielectric thickness, dielectric constant and line width will also affect the input matching circuit as well and so the experiment was then repeated with a 1.2:1 VSWR mismatch inserted at the input in addition to the mismatch at the output. The procedure that was adopted was to first set the output tuner to the worst-case power position and then a 1.2:1 VSWR tuner was inserted at the input and varied over the full 360^0 and then repeated, but this time with the output tuner set to the best-case power position. However, adding a tuner at the input had almost no additional effect on the power and gain variation. The full results are given in Table 5.

Test Condition	Gain (dB)	Power Output (W)
No Mismatch	8.1	175
1.2:1 VSWR Mismatch at o/p Worst-Case	7.8	163
1.2:1 VSWR Mismatch at i/p and o/p Worst-Case	7.8	162
1.2:1 VSWR Mismatch at o/p Best-Case	8.3	180
1.2:1 VSWR Mismatch at i/p and o/p Best-Case	8.3	181

TABLE 5: Effect of mismatch on power output.

IGN2731M180

A similar analysis to that above was undertaken for this 180W GaN on SiC transistor that operates over the same frequency range with almost identical output power. The test fixture for this part, which is shown in Figure 7, uses the same PCB board material as the bipolar part does so that tables 1-4 apply in this case also. However, the major difference between this GaN transistor and the bipolar transistor is that a full non-linear electrothermal model is available for the part, and this means that the effect of tolerances can be determined during the design phase using CAD software such as Microwave Office or ADS without the need to manufacture any hardware or make any measurements. The ability to simulate the effects of tolerances in software facilitates design centering during the design phase.

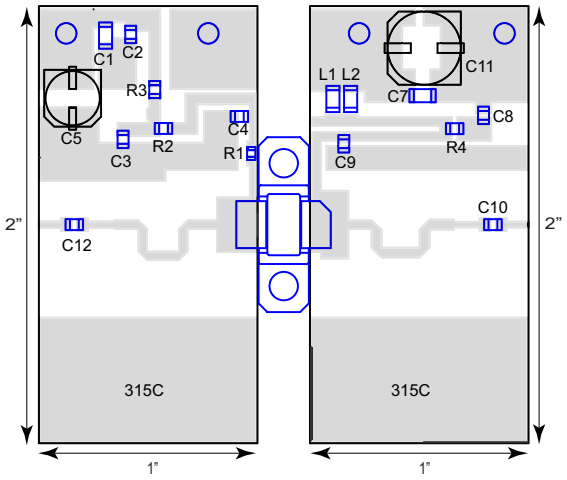

FIGURE 7: Test fixture for IGN2731M180.

Figure 8 shows the effect of making the microstrip line widths for both the input and output networks +/- 3 mils wider than nominal, while Figure 9 shows the effect of varying both substrate thicknesses by +/- 1.5 mils around the nominal 25 mils thickness.

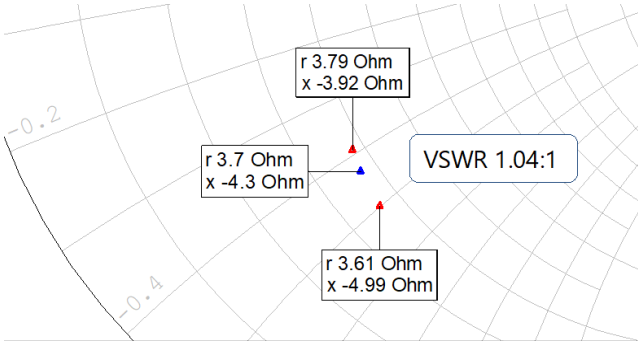

FIGURE 8: Microstrip line widths varied by +/- 3 mils around nominal with ε_r = 10.2 and thickness = 25 mils.

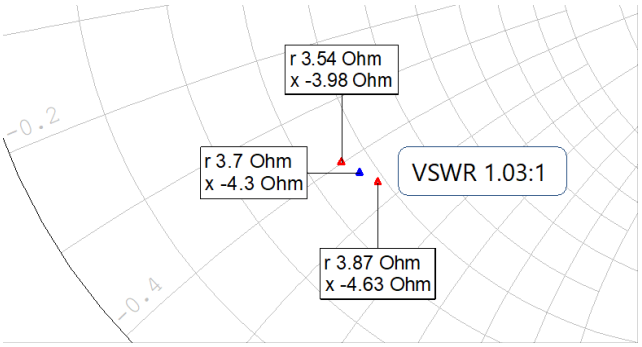

FIGURE 9: Substrate thickness varied by +/- 1.5 mils around nominal 25 mils thickness with ε_r = 10.2 and all microstrip lines having their intended width.

Figures 10 shows the effect of varying the dielectric constant of both substrates by +/- 0.25, while Figure 11 shows the worst case scenario when line width, substrate thickness and dielectric thickness are varied simultaneously. The worst case occurs when the substrate thickness is greatest, dielectric constant lowest and line widths narrowest, and *vice versa.*

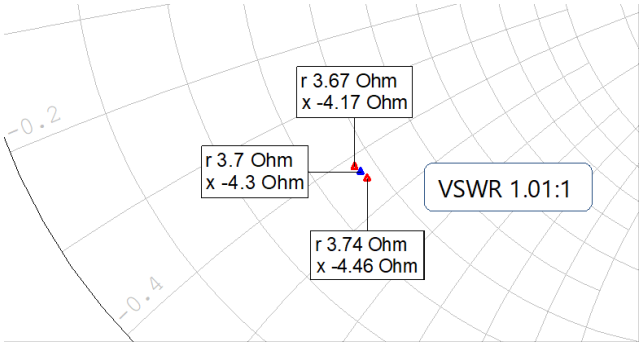

FIGURE 10: Dielectric constant varied by +/- 0.25 around nominal value of 10.2 with thickness = 25 mils and all microstrip lines having their intended width.

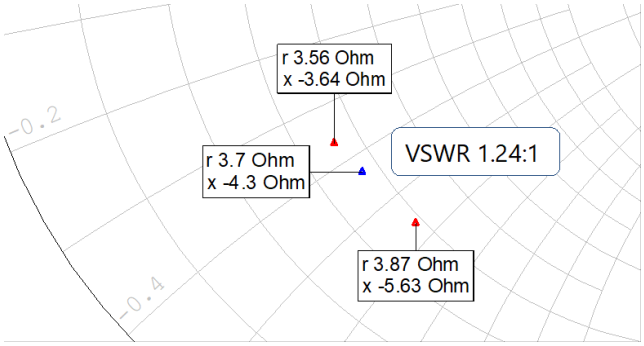

FIGURE 11: Worst-case scenario.

Finally, Figure 12 shows the effect of the two worst-case scenarios on the calculated RF power output and gain. With an RF input power of 10W (40 dBm) then the calculated nominal output power and gain is 197.6 W and 12.96 dB, respectively, but these values can vary between 179 W, 12.5 dB and 209 W, 13.2 dB if the worst-case tolerances are taken into account.

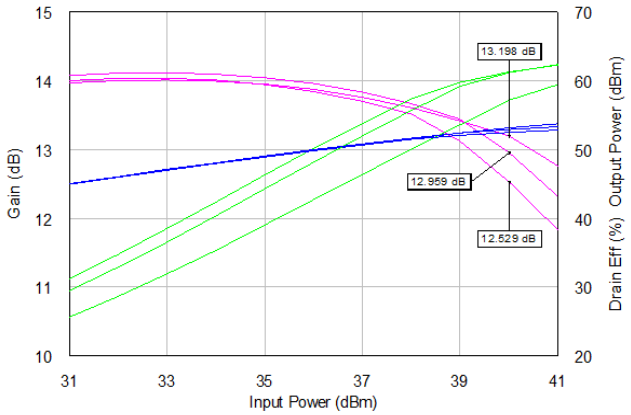

FIGURE 12: Effect of worst-case tolerances on the gain and power output of IGN2731M180 performance.

CONCLUSIONS

This Application Note has considered the effects of PCB tolerances on the performance of a bipolar transistor that was investigated experimentally as well as on a GaN transistor that was determined using Integra's non-linear model for the part. It has been shown that a mismatch as low as 1.2:1 due to the actual PCB differing from its nominal specifiaction due to tolerances can easily result in a variation of up 0.5 dB in gain and, consequently, a +/-10% variation in output power.

REFERENCES

1. https://www.everythingrf.com/rf-calculators/microstrip-impedance-calculator