

S-Band, GaN/SiC, RF Power Transistor

2.7 - 3.1 GHz | 50 W typ | 50 % Efficiency typ | 15 dB Gain typ | 100 V | 100 µs Pulse Length, 10% Duty Cycle

IGN2731M50HV and IGN2731M50HVS are high power GaN-on-SiC RF power transistors that have been designed to suit the unique needs of S band radar systems. They operate over the complete 2.7 - 3.1 GHz frequency range. Under 100 μ s, 10% duty cycle pulse conditions, they supply a minimum of 50 W of peak output power. They operate from a 100 V supply voltage. For optimal thermal efficiency, the transistors are housed in a metal-based package with an epoxy-sealed ceramic lid.





FEATURES

- GaN on SiC HEMT Technology
- Output Power >50W
- Pre-matched Input Impedance
- High Efficiency up to 60%
- 100% RF Tested Under 100μs, 10% duty cycle pulse conditions
- RoHS and REACH Compliant

APPLICATIONS

• S band Radar Systems

Table 1. RF Electrical Characteristics in Broadband Test Fixture (Case temperature = 30 °C unless otherwise stated)

Parameter	Symbol	Min	Тур	Max	Units	Test Conditions
Gain	G		15		dB	P _{out} = 50W
Drain Efficiency	η		50		%	f = 2.7, 2.9, 3.1 GHz
Pulse Droop	D	-	-0.4		dB	100μs pulse length, 10% duty cycle
Load Mismatch Stability	VSWR-S		2:1			V = 100V L = 25mA
Limited VSWR Withstand 100% test	VSWR-LMT		3:1			$V_{DS} = 100V, I_{DS} = 25mA$

Note: Consult Integra Technologies Application Note 001 for information on how RF output power and pulse droop are measured.



Table 2. Absolute Maximum Ratings (Not Simultaneous)

Parameter	Symbol	Value	Units	Test Conditions
DC Drain-Source Voltage	V _{DS}	350	V	25 °C
DC Gate-Source Voltage	V _{GS}	-8 to +1.0	V	25 °C
DC Drain Current	I _D	8	А	25 °C
DC Gate Current	I _G	8	mA	25 °C
RF Input Power	P _{RF,IN}		W	25 °C
Operating Channel Temperature	T _J	-55 to +225	°C	
Storage Temperature	T _{stg}	-62 to +150	°C	
Soldering Temperature	T _{SOLDER}	260 for 10s	°C	

Note: Operation outside the limits given in this table may cause permanent damage to the transistor

Table 3. DC Electrical Characteristics (Case temperature = 25 °C unless otherwise stated)

Parameter	Symbol	Min	Тур	Max	Units	Test Conditions
Gate Pinch-Off Voltage	V _P	-5.0			V	$V_{DS} = 100V, I_{DS} = 1mA$
Quiescent Gate Voltage	V _Q		-2.8		V	V _{DS} = 100V, I _{DS} = 25mA

Table 4. VSWR Impedance Mismatch Ruggedness (Case temperature = 30 °C unless otherwise stated)

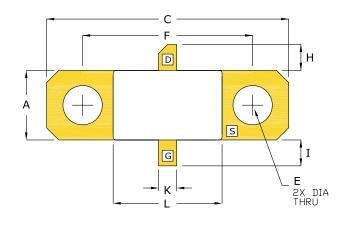
Parameter	Symbol	Тур	Test Conditions
Impedance Mismatch Ruggedness	VSWR	10:1 All phases	$P_{OUT} = 50W$ f = 2.7, 2.9, 3.1 GHz 100µs pulse length, 10% duty cycle $V_{DS} = 100V$, $I_{DS} = 25mA$

Table 5. Thermal Resistance (Case temperature = 85 °C unless otherwise stated)

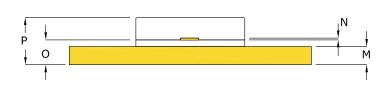
Parameter	Symbol	Тур	Test Conditions
Peak Thermal Resistance, Channel to Case	R _{TH}	TBD	$P_{DISS} = 50W$ 100 μ s pulse length, 10% duty cycle $V_{DS} = 100V$



PACKAGE PL32A2

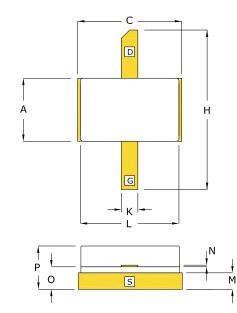


	INCHES	<u> </u>	MILLIMETERS	
MIG	MIN MAX		MIN	MAX
Α	0.225	0.235	5.72	5.97
В				
С	0.795	0,805	20.19	20.44
E	0.125	0.135	3.18	3.43
F	0.557	0.567	14.14	14.40
Н	0.093	0.107	2.36	2.72
Ι	0.093	0.107	2.36	2.72
J				
К	0.055	0.065	1.40	1.65
L	0.357	0.363	9.07	9,22
М	0.055	0.065	1.40	1.65
N	0.004	0,006	0.10	0.15
	0.077	0.087	1.96	2.21
Р	0.151	0.174	3,84	4.42



PIN :	SCHEDULE
D	DRAIN
S	SOURCE
G	GATE

BOLT-DOWN FLANGE OPTION IGN2731M50HV



	INCHES	3	MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.225	0.235	5.72	5.97
В				
С	0.375	0.385	9.53	9.78
Ε				
F				
Н	0.552	0.612	14.02	15.54
I	-			
J				
K	0.055	0.065	1.40	1.65
L	0.357	0.363	9.07	9.22
М	0.055	0.065	1.40	1.65
N	0.004	0.006	0.10	0.15
	0.077	0.087	1.96	2.21
Р	0.151	0.174	3.84	4.42

EARLESS FLANGE OPTION IGN2731M50HVS



ESD & MSL Rating

Parameter	Rating	Standard
ESD Human Body Model (HBM)	TBD	ESDA/JEDEC JS-001-2012
ESD Charged Device Model (CDM)	TBD	JEDEC JESD22-C101F
Moisture Sensitivty Level (MSL)	Unlimited Shelf Life	IPC/JEDEC J-STD-020

RoHS Compliance

Integra Technologies, Inc declares that its GaN and LDMOS Transistor Products comply with EU Directive 2011/65/EU on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863/EU.

REACH Compliance

Integra Technologies supports EU Regulation number 1907/2006 concerning the Registration, Evaluation, Authorization, and Restriction of Chemicals (REACH) as these apply to Integra semiconductor products, development tools, and shipping packaging.

In support of the REACH regulation, Integra will:

- •Inform customers and recipients of Integra product if they contain any substances that are of very high concern (SVHC) per the European Chemical Agency (ECHA) website.
- •Notify ECHA if any Integra product that contains any SVHCs which exceed guidelines for REACH chemicals by weight per part number and for total content weight per year for all products produced in or imported to the European market.
- •Cease shipments of product containing REACH Annex XIV substances until authorization has been obtained.
- •Cease shipment of product containing REACH Annex XVII chemicals when restrictions apply.

Integra has evaluated its materials, BOMs, and product specifications and product and has determined that this transistor conforms to all REACH and SVHC regulations and guidelines. Integra has implemented actions and control programs that will assure continued compliance.

Disclaimer

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DEFINITIONS:

DATA SHEET STATUS

Advanced Specification - This data sheet contains Advanced specifications.

Preliminary Specification - This data sheet contains specifications based on preliminary measurements and data.

Final Specification - This data sheet contains final product specifications.

MAXIMUM RATINGS Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.

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