INTEGRA
RF POWER DEVICES

Thermal Analysis of Integra's GaN on SiC Transistors

INTRODUCTION

The temperature of the die inside our packaged transistors determines the Median Time to Failure (MTF) as well as the RF gain and power output. All these parameters use the highest temperature within the die as the reference. There are several techniques available for measuring the temperature at the surface of the die such as Infra-Red (IR) microscopy, thermoreflectance measurement and Raman scattering. However, the highest temperature in the die occurs not at the surface but in the channel beneath metal layers and so it cannot be directly measured. Consequently, it is necessary to perform a Finite Element Analysis (FEA) of the die as mounted inside a package to calculate the peak temperature. The FEA analysis determines the temperature everywhere within the die and so the calculated surface temperature is compared with the measured surface temperature to validate the model. The FEA analsysis can be performed using software programs such as ANSYS or TCAD; Integra uses the latter.

FINITE ELEMENT ANALYSIS

Figure 1 shows the thermal resistance for Integra's GaN on SiC transistor IGN2731M180 calculated using a finite element analysis as a function of time following the application of a single 180 W, 100 s pulse with the underneath side of the transistor flange held at +85 ^{0}C, the flange being Tungsten-Copper in this instance. This transistor has a minimum efficiency of 50 % so 180 W of dissipated power corresponds to an RF output power of at least 180 W (the small adverse effect of the finite RF gain has been ignored in this calculation). Most GaN on SiC transistors have an MTF > 10^{6} hours provided the peak channel temperture is < 225 ^{0}C. From Figure 1 it can be determined that the maximum permitted pulse length is around 100 μs to keep the channel temperature below 225 ^{0}C with 180W of dissipated power. Of course, in a practical application there is usually a pulse train with a finite duty cycle rather than a single isolated pulse. It might be thought that provided the duty cycle was <50% then the device would cool down to ambient between pulses and so the data in Figure 1 could be used for any duty cycle < 50%. However, this is untrue, Reference [1] has proven analytically in a very elegant way that the cool down time is much longer than the

heat up time.

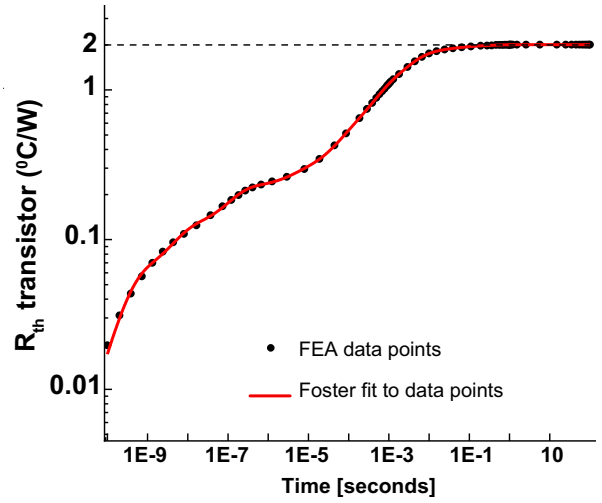

FIGURE 1: Thermal resistance versus time following the application of a single 180W pulse for 100 s with the underneath side of the flange held at 85 ^{0}C.

So how do you determine the effect of the duty cycle on peak channel temperature knowing only the response to a single isolated pulse? This is a two-step process which begins by firstly fitting a Foster network to the calculated temperature response shown in Figure 1 as discussed in References [1, 2]. Foster networks have their origin in network synthesis [3] as a means of realizing an arbitrary impedance expressed as a ratio of two polynomials, but here they are used to realize a numerical impedance. Each layer in the complete packaged transistor will have a thermal resistance between its top and bottom surfaces as well as a thermal capacitance which is in parallel with the thermal resistance. Each layer in the structure is thermally in series and so it is natural to attempt to fit a series connection of parallel RC elements (i.e. a Foster network) to the FEA-calculated data. It has been found that a 5-term Foster network provides an excellent fit to the calculated data as shown in Figure 1. The numerical curve fit can be easily undertaken using the pre-existing routines in Matlab [4]. Since all of the parallel RC networks are in series, then the same impedance is realized regardless of their order and so they have no physical relation to any region within the transistor, they are purely a numerical fit to the data.

The second step is to calculate the resulting temperature with a finite duty cycle, either by performing a time domain simulation in SPICE, or by using the closed-form analytic solution given in Reference [1] which is shown below. The analytic solution is ideal for a simple repetitive single pulse, whereas SPICE can handle very complex waveforms as discussed in the next section. It is also possible to use Microwave Office or ADS to perform the time domain simulation, but Integra recommends using LT Spice which is free software available from Analog Devices [5] as the most appropriate sofware program for this task.

The peak thermal resistance R(t, d) for any finite duty cycle is given by Equation (1):

$$R(t,d) = \sum_{i=1}^{m} R_i \frac{1-e^{-\frac{t}{\tau_i}}}{1-e^{-\frac{t}{d\tau_i}}} \qquad (1)$$

where d is the duty cycle and R_i and $\tau_i = R_iC_i$ are the elements in a Foster fit to the calculated channel temperature in Figure 1 following the application of a single isolated pulse. The peak channel temperature is given by $T_{CH} = T_{Ambient} + P_{Diss} \times R(t, d)$. Figure 2 shows the thermal resistance as a function of pulse length for various

duty cycles obtained using equation (1) for IGN2731M180.

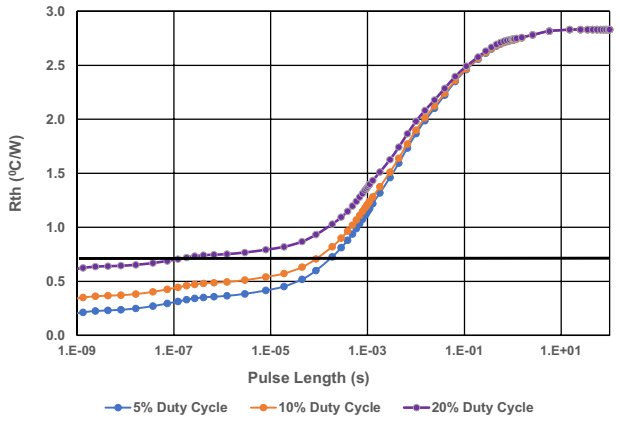

FIGURE 2: Thermal resistance vs pulse length for various duty cycles for the transistor used in Figure 1 (IGN2731M180).

USE OF LT SPICE FOR COMPLEX WAVEFORM ANALYSIS

Integra's non-linear electro-thermal models require the user to input the ambient temperature and thermal resistance (R(t, d) for the usr's pulse conditins. Figure 3 shows an example of the use of LT SPICE to calculate the peak thermal resistance in a GaN on SiC transistor with the Mode S ELM IFF pulse train. This waveform is a pulse burst of 48 x (32µs On, 18µs Off) repeated every 24 ms i.e. the long-term duty cycle is 6.4%. This waveform is simulated in LT SPICE by generating the product (element B1 in Figure 3) of two overlapping pulse trains. In this particular case, a ten-element Foster fit to calculated FEA data was used. SPICE calculates the peak voltage in response to the applied current pulse of 1A amplitude. In the thermal/electrical analogue, current represents dissipated power and voltage represents temperature. As can be seen from Figure 4a and 4b, the peak voltage (i.e. temperature rise above ambient) is 1.05V (1.05 ^{0}C) for a 1A pulse (1W dissipated power) and so the thermal resistance of this transistor operated with the Mode S ELM waveform is 1.05 ^{0}C/W.

The things to note from Figures 4a and 4b are that the transistor cools down to ambient after each pulse burst, but not between each individual pulse within the burst. Figure 4b clearly shows a steady increase in the peak temperature during the burst.

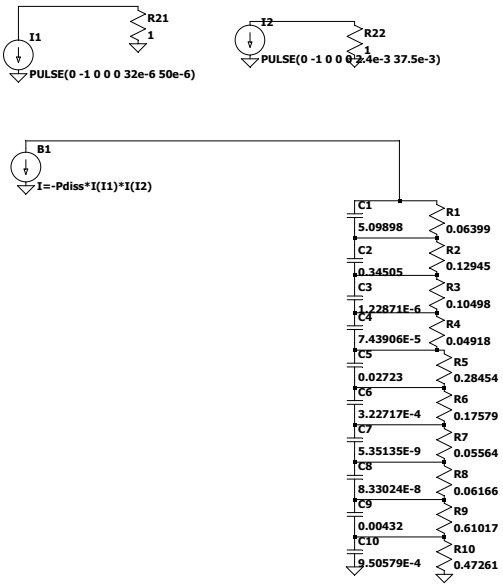

FIGURE 3: SPICE network for calculating the thermal resistance with the Mode S ELM waveform.

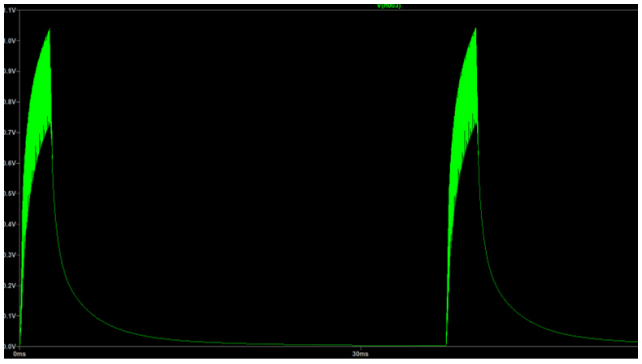

FIGURE 4a: Channel Temperature rise vs time.

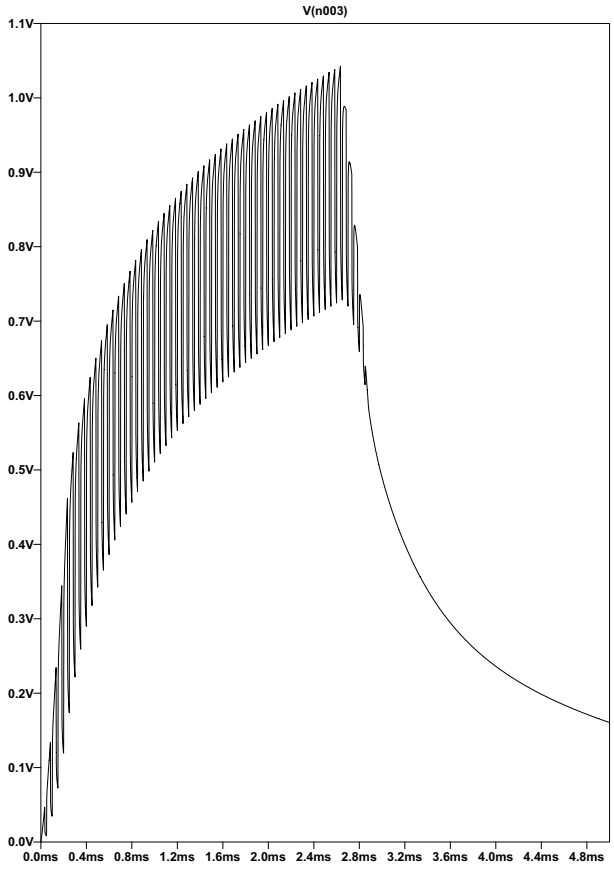

FIGURE 4b: Expanded view of Figure 4a.

However, there are two limitations that must be stated about using Foster networks to predict channel temperature. These stem from the fact that both GaN and SiC are thermally non-linear materials because their thermal conductivity and specific heat are temperature dependent, and so the Foster fit is only valid for the precise ambient temperature and power dissipation used in the finite element analysis. The Foster network is a linear network and so if the dissipated power is doubled then so too will the channel temperature double which will result in an underestimate of the true situation.

Likewise, if the ambient temperature is increased by, say, 40 ^{0}C then the channel temperature will also increase by 40 ^{0}C which, again, will under-estimate the true channel temperature. Foster networks are very useful for predicting the channel temperature for various pulse conditions, but the FEA analysis must be repeated and a new Foster network fitted if either the ambient temperature or power dissipation are varied to obtain an accurate value for channel temperature. .

OPERATION UNDER BACK-OFF

Integra's transistors are always operated in deep class A/B bias. This means that the power dissipated in the transistor varies with the RF power output, unlike class A where it is invariant. It is common for the maximum dissipated power, and hence channel temperature, to occur at some point in the back-off region rather than at maximum power poutput. Figure 5 shows a graph of dissipated power as a function of RF output power for IGN1011L1200 which is a 1200W transistor designed for Mode S ELM applications. It can be seen that the peak dissipated power, and hence channel temperature, occurs when the output power is halved to 600W. In this condition, the channel temperature rise above ambient is three times higher than it is at its rated output power of 1200W.

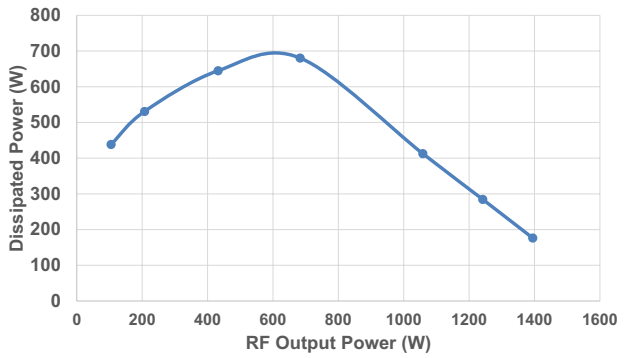

FIGURE 5: Dissipated power as a function of RF output power for IGN1011L1200.

REFERENCES

1. Application Note AND8219/D, "How to Generate Square Wave, Constant Duty Cycle, Transient Response Curves". ON Semiconductor. http://onsemi.com.

2. X. Zheng , J. Pomeroy , G. Jindal , and M. Kuball, "Temperature-Dependent Thermal Impedance Measurement of GaN-Based HEMTs Using Transient Thermoreflectance", IEEE Transactions on Electron Devices, Vol. ED-7, Feb, 2024, pp. 2367 – 2372.

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4. https://uk.mathworks.com/help/curvefit/curvefitter-app.html.

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