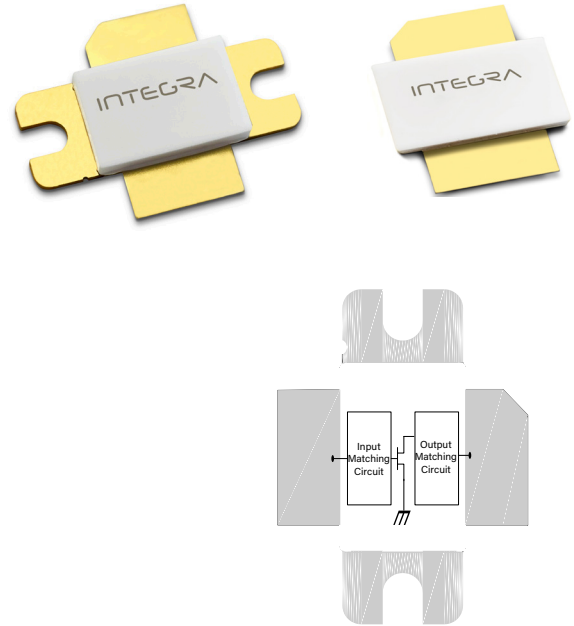


S-Band, GaN/SiC, RF Power Transistor

3.0 GHz | 3200W | 60 % Efficiency typ | 16 dB Gain typ | 125 V | 10µs Pulse Length, 1% Duty Cycle

Introducing IGN3000S2700 and IGN3000S2700S, the pinnacle of S-Band power transistors available today. Powered by Integra’s Gen4 GaN/SiC, IGN3000S2700 and IGN3000S2700S deliver an astonishing 3200W of peak output power and boast a typical power gain of 16dB at an impressive 60% drain efficiency. This powerhouse of innovation is designed for practicality and efficiency, enabling replacement of traditional vacuum electron device (VED) based amplifier systems with ease, even at megawatt power levels. Experience unparalleled improvements in system size, weight, power, cost, and complexity, paving the way for the next generation of RF amplifier system performance. Elevate your system architecture with IGN3000S2700 and IGN3000S2700S and witness the future of high-performance system amplification.



FEATURES

- ✓ Solid-State Excellence: Effortlessly replace VEDs with cutting-edge solid-state technology.
- ✓ Advanced GaN/SiC Technology: Powered by Integra’s Gen4 GaN/SiC for superior performance.
- ✓ Impressive Efficiency: Achieve a remarkable 60% drain efficiency for optimal operation.
- ✓ Unbeatable Output Power: Delivering 300% more output power than competitors.
- ✓ Streamlined Design: Replace multiple legacy amplifiers with a single, powerful unit.
- ✓ Innovative Architecture: Eliminate complex power combining layers in your amplifier system.

APPLICATIONS

- Particle Accelerators and ISM Systems

Table 1. RF Electrical Characteristics (Case temperature = 30 °C unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Gain	G		15		dB	$P_{OUT} = 2700W$ $f = 3.0 GHz$ 10µs pulse length, 1% duty cycle $V_{DS} = 125V, I_{DS} = 150mA$
Drain Efficiency	η		58		%	
Pulse Droop	D		-0.1		dB	
Input Return Loss	IRL		21		dB	
VSWR Mismatch Stability	VSWR-S	2:1				
VSWR Withstand	VSWR-LMT	5:1				

Note: Consult Integra Technologies Application Note 001 for information on how RF output power and pulse droop are measured.

Table 2. Absolute Maximum Ratings (Not Simultaneous)

Parameter	Symbol	Value	Units	Test Conditions
DC Drain-Source Voltage	V_{DS}	350	V	25 °C
DC Gate-Source Voltage	V_{GS}	-8 to +1	V	25 °C
DC Drain Current	I_D	72	A	25 °C
DC Gate Current	I_G	14.4	mA	25 °C
RF Input Power	$P_{RF,IN}$	135	W	25 °C
Operating Channel Temperature	T_{CH}	-55 to +225	°C	
Storage Temperature	T_{STG}	-55 to +150	°C	
Soldering Temperature	T_{SOLDER}	260 for 60s	°C	

Note: Operation outside the limits given in this table may cause permanent damage to the transistor

Table 3. DC Electrical Characteristics (Case temperature = 25 °C unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Gate Pinch-Off Voltage	V_P	-5.0			V	$V_{DS} = 125V, I_{DS} = 1mA$
Quiescent Gate Voltage	V_Q		-4.0		V	$V_{DS} = 125V, I_{DS} = 150mA$

Table 4. Thermal Resistance (Case temperature = 85 °C unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Peak Thermal Resistance, Channel to Case	R_{TH}		0.044		°C/W	$P_{diss} = 1955W$ 10µs pulse length, 1% duty cycle $V_{DS} = 125V$

TYPICAL PERFORMANCE

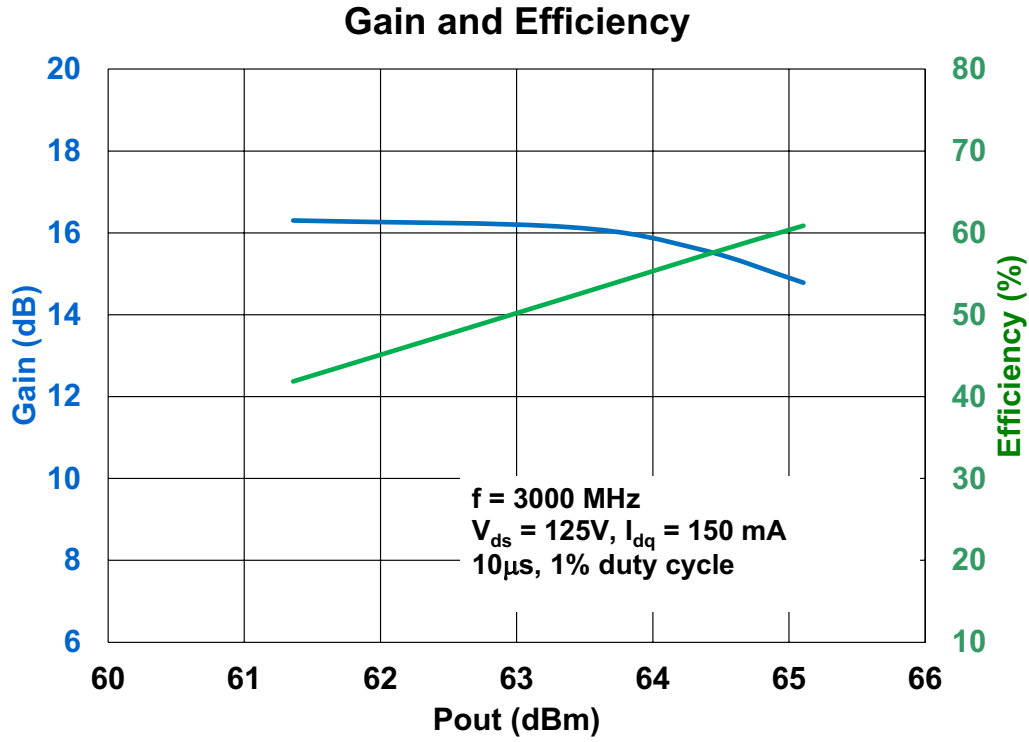
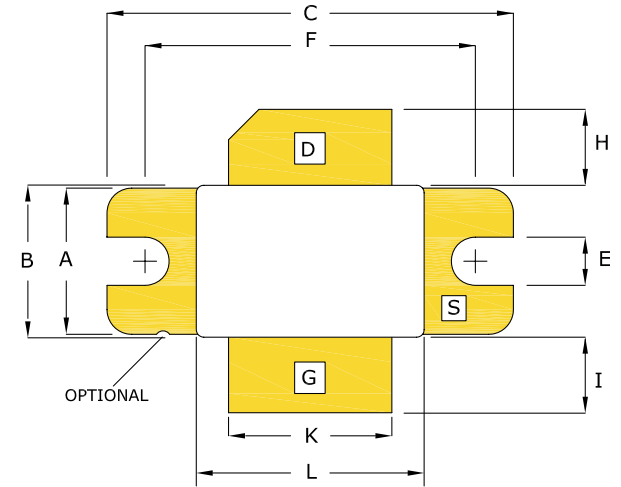


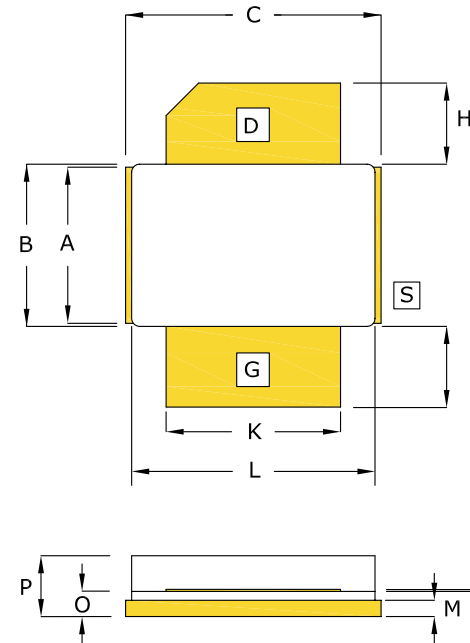
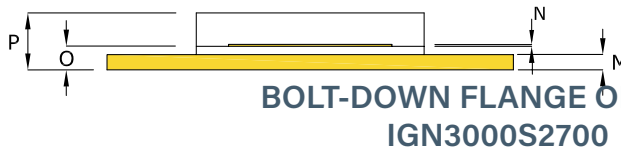
Figure 1

PACKAGE PL64B1



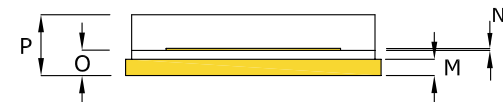
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.380	0.390	9.65	9.91
B	0.395	0.405	10.03	10.29
C	1.065	1.075	27.05	27.31
E	0.123	0.133	3.12	3.38
F	0.865	0.875	21.97	22.23
H	0.180	0.220	4.57	5.59
I	0.180	0.220	4.57	5.59
J	--	--	--	--
K	0.425	0.435	10.80	11.05
L	0.595	0.605	15.11	15.37
M	0.035	0.045	0.89	1.14
N	0.004	0.006	0.10	0.15
O	0.057	0.067	1.45	1.70
P	0.142	0.175	3.61	4.45

PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.380	0.390	9.65	9.91
B	0.395	0.405	10.03	10.29
C	0.625	0.635	15.88	16.13
E	--	--	--	--
F	--	--	--	--
H	0.180	0.220	4.57	5.59
I	0.180	0.220	4.57	5.59
J	--	--	--	--
K	0.425	0.435	10.80	11.05
L	0.595	0.605	15.11	15.37
M	0.035	0.045	0.89	1.14
N	0.004	0.006	0.10	0.15
O	0.057	0.067	1.45	1.70
P	0.142	0.175	3.61	4.45

PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE



**EARLESS FLANGE OPTION
IGN3000S2700S**

ESD Rating

Parameter	Rating	Standard
ESD Human Body Model (HBM)	TBD	ESDA/JEDEC JS-001-2012
ESD Charged Device Model (CDM)	TBD	JEDEC JESD22-C11F
Moisture Sensitivity Level (MSL)	Unlimited Shelf Life	IPC/JEDEC J-STD-020

RoHS Compliance

Integra Technologies, Inc declares that its GaN and LDMOS Transistor Products comply with EU Directive 2011/65/EU on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863/EU.

REACH Compliance

Integra Technologies supports EU Regulation number 1907/2006 concerning the Registration, Evaluation, Authorization, and Restriction of Chemicals (REACH) as these apply to Integra semiconductor products, development tools, and shipping packaging.

In support of the REACH regulation, Integra will:

- Inform customers and recipients of Integra product if they contain any substances that are of very high concern (SVHC) per the European Chemical Agency (ECHA) website.
- Notify ECHA if any Integra product that contains any SVHCs which exceed guidelines for REACH chemicals by weight per part number and for total content weight per year for all products produced in or imported to the European market.
- Cease shipments of product containing REACH Annex XIV substances until authorization has been obtained.
- Cease shipment of product containing REACH Annex XVII chemicals when restrictions apply.

Integra has evaluated its materials, BOMs, and product specifications and product and has determined that this transistor conforms to all REACH and SVHC regulations and guidelines. Integra has implemented actions and control programs that will assure continued compliance.

Disclaimer

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DEFINITIONS:

DATA SHEET STATUS

Advanced Specification - This data sheet contains Advanced specifications.

Preliminary Specification - This data sheet contains specifications based on preliminary measurements and data.

Final Specification - This data sheet contains final product specifications.

MAXIMUM RATINGS Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.

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