

Transistor Installation Instructions

INTRODUCTION

When inserting high power RF transistor packages into amplifier circuits there are two important objectives. Firstly, removing heat and, secondly, providing a long-term reliable solder joint to the printed circuit board.

From a thermal perspective, the objective with any method of attachment is to achieve the best metal-to-metal contact between the underneath side of the flange and the heatsink i.e. minimizing any voiding and, if used, minimizing the amount of any intermediate material. Any intermediate material such as solder, thermal grease or thermal pad must have the highest possible thermal conductivity and be as thin as possible. Integra's recommended mounting method to achieve the above objectives is to use full solder attach, but ordinary bolt-down using a thermal pad or silicone grease can also be used. Silicone grease has a very poor thermal conductivity compared with the transistor flange or the heatsink and so the only purpose for using grease is to fill in any air gaps that might otherwise exist between the flange and the heatsink. Consequently, only a thin film of silicone grease should ever be used, its thickness should never be

such that it interferes with the direct metal-to-metal contact that would otherwise occur if no silicone grease was used. Integra prefers the use of a very high thermal conductivity thermal pad which molds its shape into any irregularities in the flatness of either the transistor flange or the baseplate rather than the use of silicone grease. Finally, it should be noted that while epoxy attachment of components to the surface of printed circuit boards is widely used for low-power components, it must never be used for Integra's RF power transistors since the dissipated power is too high. Even the best silver-loaded epoxies have only half the thermal conductivity of tin-lead solder.

GOLD REMOVAL AND TINNING

1. The plating on transistor packages is normally a minimum of 150 μ " of Au over 100 μ " minimum of Ni. However, the gold can be as thick as 200 μ " and so gold embrittlement will be a concern if the solder joint is less than .010" thick and is >2% Au by volume when using Sn62 or Sn63 solder without gold removal from the leads prior to lead tinning.

- The gold can be removed from leads either by dipping the leads into a pot of molten Sn/Pb solder, or by manually applying solder to the bottom of the leads and removing it with a soldering iron. If using a solder pot for gold removal then the gold content in the pot has to be monitored and maintained at a low level (<1% by volume). The gold removal should cover the bottom of the lead to within 0.020" of the ring frame. In both cases, it is desirable to pre-heat the transistor to about 60 °C (for Sn63) before removing the gold.
- A fixture is required for tinning to hold the transistors and achieve the correct lead coverage, as well as protect the flange from solder splashes. Tinning is often performed on the top and bottom of the transistor leads with a soldering iron. The tip temperature should be < 350 °C for Sn63 solder. It is desirable to pre-heat the transistor to about 60 °C to minimize the time above reflow and reduce the heat required from the iron. It also helps the entire lead to reflow. The tinning on the bottom of the lead should cover up to within 0.020" of the ring frame. The height of the solder should be kept to less than 0.002" on the bottom of the lead to prevent mechanical interference when inserting the transistor into the well. Figure 1 shows an example of a poorly tinned transistor lead. The distance from the lead-frame to the tinning is too great and inconsistent. A large distance will place a series inductance between the transistor and the PCB matching circuit, and this inductance will cause the incorrect impedance to be presented to the transistor.

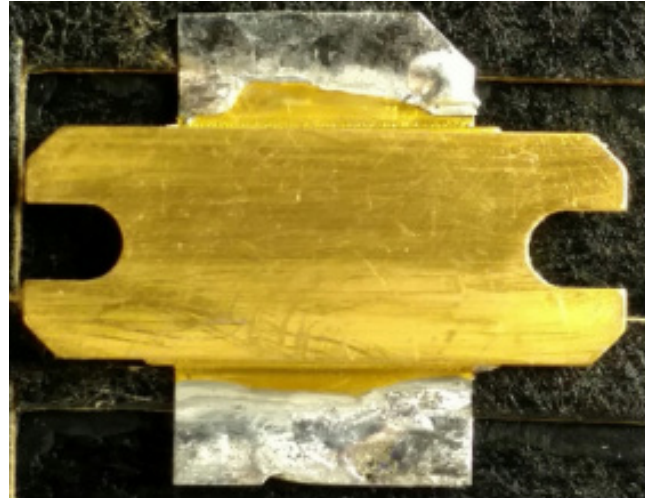


FIGURE 1: Example of a transistor with poor lead tinning coverage.

RECOMMENDATIONS FOR TRANSISTOR SOLDER ATTACHMENT

- Integra recommends soldering the flange and the transistor leads using a reflow oven for the best mechanical and electrical attachment of a transistor to an amplifier or pallet. The flange should be soldered using a 0.010" solder preform coated with no-clean flux. The lead solder pads should have 0.015" solder paste applied with a solder stencil. The nominal well depth should be the same as the nominal lead height since the transistor will be raised about 0.010" due to the preform under the flange.
- It is important that the maximum time/temperature ratings of the transistor be observed for all assembly operations:
 - Maximum Temperature= 245 °C
 - Maximum Time above 240 °C = 30 Seconds
 - Maximum Time above 217 °C = 150 Seconds
 - Ramp up rate $dTemp/dt < 3 \text{ }^{\circ}\text{C}/\text{sec}$

Ramp down rate $dTemp/dt < 6 \text{ }^{\circ}\text{C}/\text{sec}$
Total process time $T_{\text{room}} \text{ to } T_{\text{peak}} < 8 \text{ minutes}$
Maximum number of reflows = 3

RECOMMENDATIONS FOR TRANSISTOR BOLT-DOWN ATTACHMENT

1. It is not recommended that the gold flange be in direct contact with bare aluminum due to possible galvanic corrosion. The electrode potential of Au = +1.5V while Al = -1.67V. Clear anodizing is often used to protect the aluminum, but this degrades the conductivity of the aluminum. A common plating that is compatible with Au plated transistor flanges is to specify an ENIG (Electro-less Nickel, Immersion Gold) finish plating in the transistor well. A typical ENIG specification is to plate Electro-less Nickel 50-150 μm thick, followed by Immersion Gold Plating 3-8 μm thick. This provides a compatible surface finish for both bolt-down and solder transistor attachment.
2. The flatness of the mating surface should be 0.4 mils/in maximum with a surface finish of 0.02 mils to have the best possible contact between the heat sink and the device.
3. Bolt-down can be achieved using either a thermal pad or thermal grease. The recommended thermal pad is Panasonic Carbon Graphite (PGS) sheet [1] for mounting devices. Our recommended sheet is 0.001" thick, (180 x 230 x 0.025 mm) P/N: EYGS182303. The thermal pad preform should be die-cut to the shape of the nominal dimensions of the flange with a tolerance of +/-0.005", including cut-outs for the screw holes.
4. Inspect the transistor well and the transistor flange for debris, solder splash, or bumps. Remove these if necessary.
5. Install the die-cut PGS 0.001" thick thermal pad preform in the transistor well. Make sure the preform is centered in the well.
6. If using silicone grease rather than a thermal pad then Integra recommends Wakefield 120 [2] or equivalent. Apply only a thin smear of grease and ensure that it covers the whole of the flange and not just under the center of the device. This is important to ensure that no excess bowing force is applied to the flange during bolt-down as this can lead to cracking of die and substrates inside the package. Figure 2 shows an example of a transistor that failed because of incorrect application of thermal grease. Too much grease was applied in the center with none where the screw holes are located which caused the flange to bow during bolt-down and cracked a substrate inside the package. When correctly applied, the silicone grease should flow during bolt-down to fill in the voids that would otherwise exist due to surface flatness imperfections and leave the maximum amount of direct metal to metal contact.



FIGURE 2: Example of a transistor that failed due to incorrect application of silicone grease.

7. Once the pad has been inserted or silicone grease applied then insert the transistor in the well.
8. Insert the screws and use both a flat and a spring washer.
9. Screw down the transistor to the heat sink using a torque-limiting screwdriver. If the screw thread size is 4-40 UNC, then 4.5 to 5 in-lbs of torque is recommended.
10. The torque has to be applied in at least two steps:
Finger tighten to 0.05 N-m (0.4 in-lbs) on each side and then gradually tighten each side using a controlled torque screwdriver until 0.6 N-m (5.4 +/- 0.8 in-lbs) is achieved on each side.

LEAD ATTACHMENT TO THE PRINTED CIRCUIT BOARD

1. The height of the solder joint from the surface of the PCB to the bottom of the transistor lead is critical for creating a reliable solder joint and reducing stress on the transistor lead. A minimum of 0.005" joint height should be maintained if gold removal from the leads is used and a minimum of 0.010" if gold removal from the leads is not performed. Table 1 shows the required well depth for tinned and un-tinned transistor leads in order to maintain the proper minimum joint height.
2. The recommended way for solder attachment is to screen print Sn63 solder onto the solder lands prior to installing the transistor in the well with a 0.015" thick stencil. It is also desirable to put a 0.05-0.010" wide strip of solder mask along the edge of the transistor well to prevent solder from falling into the well. Figure 3 shows the solder mask border around the solder pad for the transistor leads. The solder paste can be applied manually using a syringe if using a stencil is not an option. The solder paste needs to cover the entire

solder land, especially along the edge of the transistor well and it should be 0.015" thick. The soldering can be performed using a hot-air reflow oven, a hot-air knife, or a soldering iron around the perimeter of the joint. A more consistent solder joint can be obtained if the pallet or amplifier is heated prior to soldering the leads. The recommended temperature is 50-60°C while soldering the transistor leads. No downward pressure should be applied to the lead with the soldering iron. The solder joint height should be maintained out to the end of the lead. Solder wire with no-clean flux can be used to add solder around the perimeter of the joint if voiding is visible. Solder wire with no clean flux can be used to solder the leads, if solder paste is not an option.

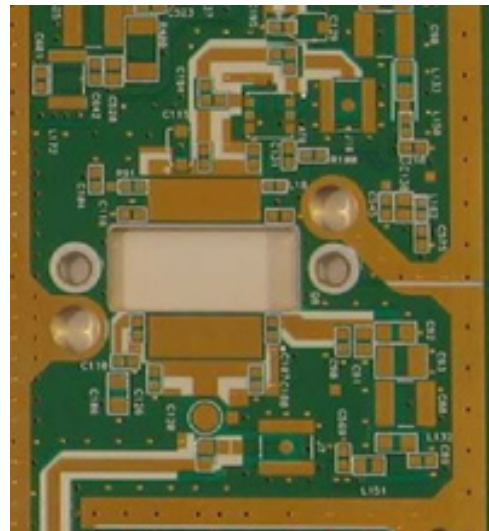


FIGURE 3: Solder Mask Border

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Well Depth (mils)			Lead Height (mils)			Flange Joint Height (mils)	Lead joint Height (mils)			
Mean	Tolerance	Std Dev	Mean	Tolerance	Std Dev		Mean	Std Dev	-3 Std Dev	+3 Std Dev
74	2	0.67	85	6	2	0	11	2.11	4.68	17.32
69	2	0.67	85	6	2	0	16	2.11	9.68	22.32

TABLE 1: Proper Transistor Well Depth for Tinned and Untinned Leads Determined by RSS Method

CONCLUSION

This Application Note has given recommendations on how to attach Integra’s RF power transistors into amplifiers and pallets to obtain the best thermal and electrical contact as well as produce a reliable solder joint to the printed circuit board. If additional information is required then please contact Integra Technologies.

REFERENCES

1. <https://industrial.panasonic.com/cdbs/www-data/pdf/AYA0000/AYA0000C27.pdf>
2. <http://www.wakefield-vette.com/resource-center/downloads/brochures/thermal-management-accessories-wakefield.pdf>