Part Number: ILD1214M10

Integra
TECHNOLOGIES, INC.

L-Band Radar RF Power LDMOS Transistor

The high power transistor part number ILD1214M10 is designed for L-Band radar operating at 1200-1400 MHz. This LDMOS FET device under 300us, 10% pulse format supplies a minimum of 10-15 watt of peak pulse power. All devices are 100% screened for large signal parameters.

TYPICAL DATA *TYPICAL DATA* *TYPICAL DATA*

Device	Freq (MHz)	P_{IN} (W)	IRL (dB)	P_{OUT} (W)	G_P (dB)	d_G (dB)	I_d (A)	η_d (%)	Droop (dB)	VSWR S	VSWR LMT
5037277-1	1200	1	-8.40	19.30	12.86		1.320	48.7	0.00	P	P
	1300	1	-18.00	19.96	13.00	0.73	1.280	52.0	-0.01	P	P
	1400	1	-10.80	16.89	12.28		1.110	50.7	-0.02	P	P

V_D=30V, I_{DQ1}=10mA, Pulse Format = 300µs, 10%.

Silicon LDMOS FET
- High Power Gain
- Superior thermal stability
- Gold Metal

Class AB Operation
- Gate biased to I_{DQ}=10mA

Configuration
- Common Source

Gold Metal
- Maximum Reliability

BeO - Free Package
- Metal Based
- Epoxy Seal

Epoxy Sealed Lid
- Gross Leak Qualified

RF Test Fixture
- Broadband
- Matched to 50Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning Allowed

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FAX: 310-606-0865

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EL SEGUNDO, CA 90245-4620

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	65	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	12	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	2.4	°C/W	V_{DS}=30V, P_{OUT}=10W, I_{DQ}=10mA, PW1=300us, 10%, F=F1, F2, F3 T_F = 25±5°C
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	65	--	V	I_{DS}=10mA, V_{GS}=0V, T_F=25±5°C.
100%	Drain Leakage Current	I_{DSS}	--	1.0	uA	V_{DS}=30V, V_{GS}=0V, T_F=25±5°C.
100%	Gate Leakage Current	I_{GSS}	--	1.0	uA	V_{GS}=5V, V_{DS}=0V, T_F=25±5°C.
100%	Operating Gate Voltage	V_{GS}	2.5	4.0	V	Id=100mA, V_{DS}=5V, T_F=25±5°C.

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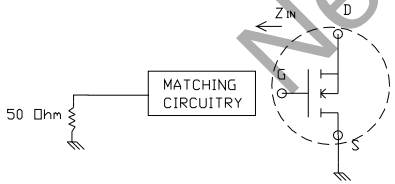
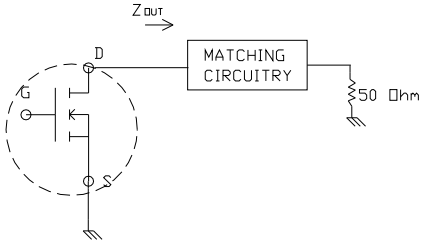
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-7	dB	Vd=V1, Pin=Pin1, Idq=Idq1, Pulse=PW1, F=F1, F2, F3, Tf=Tf1
100%	Output Power	Pout	10	25	W	Vd=V1, Pin=Pin1, Idq=Idq1, Pulse=PW1, F=F1, F2, F3, Tf=Tf1
100%	Power Gain	Gp	10	14.0	dB	Vd=V1, Pin=Pin1, Idq=Idq1, Pulse=PW1, F=F1, F2, F3, Tf=Tf1
100%	Drain Efficiency	Nd	40	75	%	Vd=V1, Pin=Pin1, Idq=Idq1, Pulse=PW1, F=F1, F2, F3, Tf=Tf1
100%	Signal Amplitude Droop	Droop	-0.5	0.5	dB	Vd=V1, Pin=Pin1, Idq=Idq1, Pulse=PW1, F=F1, F2, F3, Tf=Tf1
100%	Stability into 1.5:1 VSWR	VSWR-S	1.5:1	--	--	Vd=V1, Pin=Pin1, Idq=Idq1, Pulse=PW1, F=F1, F2, F3, Tf=Tf1 Rotate 1.5:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
100%	Load Mismatch Tolerance	VSWR-LMT	2:1	--	--	Vd=V1, Pin=Pin1, Idq=Idq1, Pulse=PW1, F=F1, F2, F3, Tf=Tf1 Rotate 2:1 output VSWR through 360° phase.
Note 1	V1=30V, Pin1=1W, PW1=300us, 10%, Idq1=10mA, F1=1200 MHz, F2=1300 MHz, F3=1400 MHz					
Note 2	Tf1=25±5°C					
Note 3	T_F = Device flange temperature.					
Note 4	Screen 'BD' = parameter qualified By Design.					

OPTIMAL IMPEDANCE CHARACTERISTICS

Frequency (MHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
1200	2.9 –j5.23	13.4 +j1.5
1300	2.68 –j4.32	12.5 –j2.9
1400	2.47 –j3.45	14.4 +j5.2
Impedance Definition		

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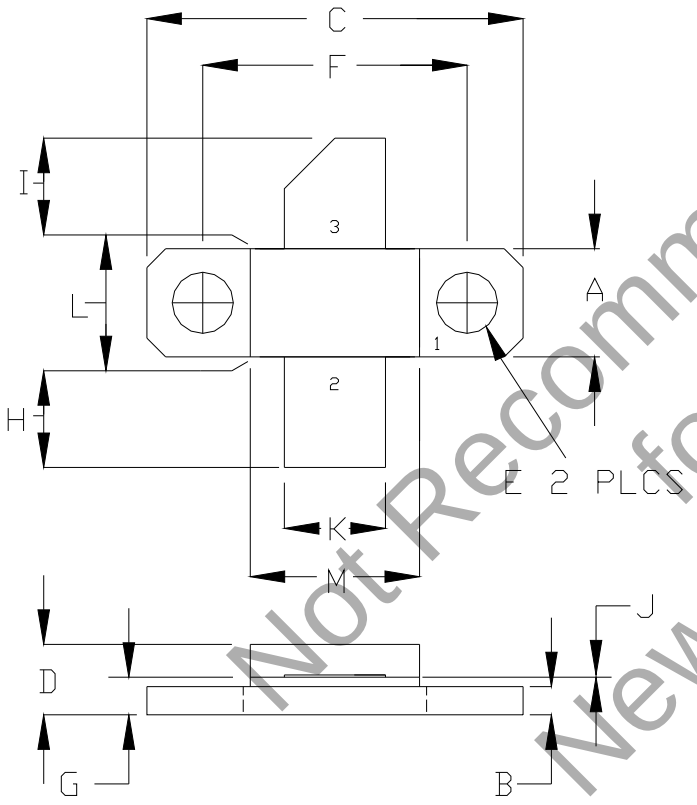
PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.225	0.235	5.71	5.96
B	0.055	0.065	1.40	1.65
C	0.795	0.805	20.19	20.44
D	0.140	0.160	3.55	4.06
E	0.125	0.135	3.18	3.43
F	0.557	0.567	14.14	14.40
G	0.077	0.087	1.95	2.20
H	0.230	0.240	5.84	6.09
I	0.230	0.240	5.84	6.09
J	0.004	0.006	0.10	0.15
K	0.210	0.220	5.33	5.59
L	0.225	0.235	5.71	5.96
M	0.355	0.365	9.01	9.27

PIN SCHEDULE	
1	SOURCE
2	GATE
3	DRAIN

NOTE: SEE BOM

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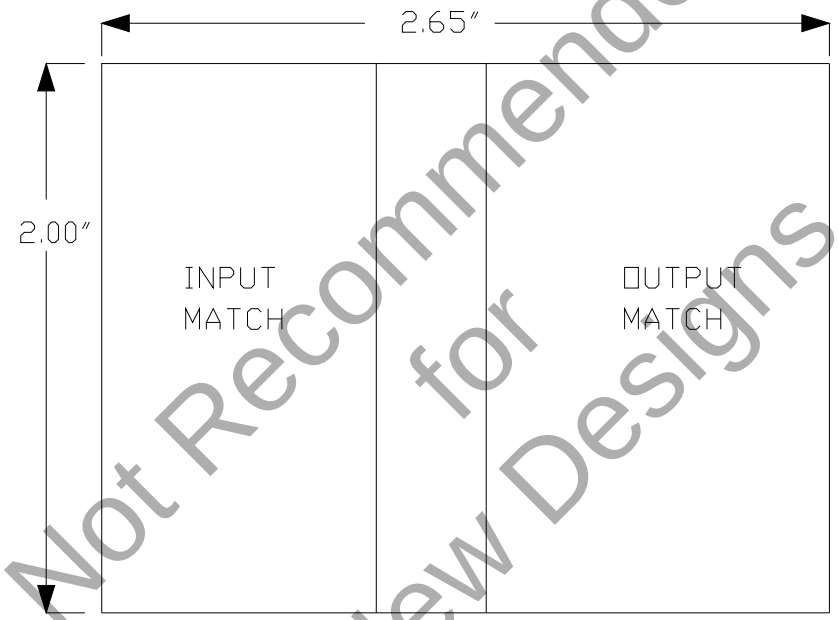
RF TEST FIXTURE



CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS

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DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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