High Power GaN Transistors

John Walker
Integra Technologies, Inc.
SCOPE

• >100W
• >1GHz
• Pulsed
AGENDA

• Technical Background
• Integra Die Manufacturing Process
• State-of-the-art GaN Products
• Conclusions
THE TECHNICAL PROBLEM

As frequency $\uparrow$
- $L_g \downarrow$ (to reduce capacitance)
- $L_{ds} \downarrow$ (to reduce parasitic series resistance)
- $V_{dsBK} \downarrow$ (Critical field remains constant)
- RF output power /mm of gate width $\downarrow$

The solution: Use a semiconductor with as high a critical field as possible
THE TECHNICAL PROBLEM (Cont.)

<table>
<thead>
<tr>
<th>Critical Field</th>
<th>Thermal Conductivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>x</td>
</tr>
<tr>
<td>GaN</td>
<td>10x</td>
</tr>
<tr>
<td>SiC</td>
<td>10x</td>
</tr>
<tr>
<td></td>
<td>y</td>
</tr>
<tr>
<td></td>
<td>y</td>
</tr>
<tr>
<td></td>
<td>3y</td>
</tr>
</tbody>
</table>

- Cannot utilise factor of 10 power advantage of GaN c.f. Si using only GaN because of thermal limitation
- Even GaN on SiC will allow only a factor of 2-3 power advantage in CW
- GaN on SiC can offer >3x Si power in pulsed applications
- NB Higher power/mm$^2$ means lower Capacitance/Watt i.e. GaN can operate to higher frequency than Si.
CW Thermal resistance of discrete single-ended transistors

$R_{\theta \text{GaN}} \approx 2.5 \times R_{\theta \text{Si LDMOS}}$

GaN is an ideal technology for pulsed applications!

16 manufacturers worldwide of pulsed GaN transistors!
IMPORTANCE OF LOW CAPACITANCE

\[ Z_{Lopt} = \frac{R_{opt}}{1 - j\omega C_{ds} R_{opt}} \]

- Re \( Z_{Lopt} \) Ω

- Capacitance, pF

- 1GHz, 1kW
- \( V_{supply} = 50V \)
Si Bipolar

- Very mature
- Very reliable
- Higher efficiency than LDMOS (class C vs class A/B) – almost as good as GaN
  - Simplest & cheapest circuits of any technology
  - Frequency extension via common-base mode
- Lowest gain
- Very non-linear
- BeO package
Si Bipolar

- Simplest & cheapest circuits of any technology

1.5kW bipolar L band
Just 2 chip capacitors
1 supply voltage

1kW LDMOS L band
10 capacitors, 1 resistor
2 supply voltages
Si Bipolar

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- Frequency extension via common-base mode

\[ f_t \propto \frac{1}{C_{in}} = \frac{1}{C_{be} + C_{bc}} \]

FETs have \( C_{ds} \) which is comparable in value to \( C_{gs} \) so no frequency extension by using common gate mode
TECHNOLOGY COMPARISON

Si Bipolar

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  - BeO package
TECHNOLOGY COMPARISON

Si LDMOS

- Very linear
- BeO-free and cheaper package
- About 2 dB more gain than bipolar but less than GaN
- Lowest efficiency
- No increase in power output compared with bipolar
TECHNOLOGY COMPARISON

GaN

- Lowest capacitance per Watt of any technology
  - Wider bandwidth and higher frequency, less ripple
- Higher optimum load impedance

- Highest power density
  - Thermal issues
- Worse linearity than LDMOS
IMPORTANCE OF LOW CAPACITANCE

\[ Z_{\text{Lopt}} = \frac{R_{\text{opt}}}{1 - j\omega C_{ds} R_{\text{opt}}} \]

Re \( Z_{\text{Lopt}} \) \( \Omega \)

- 1GHz, 1kW
- \( V_{\text{supply}} = 50V \)

Capacitance, pF
## TECHNOLOGY COMPARISON

**2.7-2.9GHz, 300µs, 10% duty cycle**

<table>
<thead>
<tr>
<th>Device</th>
<th>Technology</th>
<th>Power (W)</th>
<th>Power-Added Efficiency %</th>
<th>Gain (dB)</th>
<th>Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IB2729M170</td>
<td>Si Bipolar</td>
<td>190</td>
<td>45</td>
<td>9.5</td>
<td>36</td>
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<tr>
<td>ILD2731M140</td>
<td>LDMOS</td>
<td>180</td>
<td>40.5</td>
<td>10.5</td>
<td>32</td>
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<tr>
<td>IGN2729M250</td>
<td>GaN</td>
<td>260</td>
<td>51</td>
<td>9.5</td>
<td>36</td>
</tr>
<tr>
<td>IGN2729M800</td>
<td>GaN</td>
<td>1000</td>
<td>55</td>
<td>11</td>
<td>50</td>
</tr>
</tbody>
</table>
Integra Die Manufacturing Process

- Integra designs and manufactures its own GaN die
- Die specifically designed for **pulsed operation**
- 4” GaN on SiC (6” ready)
- 0.5µm process
- Ti/Al/Ni/Au Ohmic contacts
- Ni/Au Gate contact
- 3 mil die thickness
- Double field plate design
- No via holes
- All gold process for high reliability
- High breakdown voltage for reliable 50V operation
Die Details

- 36mm total gate periphery
- 300µm finger width
- >150W 2.7-2.9GHz
AGENDA

• Technical Background
• Integra Die Manufacturing Process
  ➢ State-of-the-art GaN Products
• Conclusions
Integra 800W S band Package Details

GaN Die

1.1”

1.23”
Integra 800W S band Results

Test Conditions:
300µs, 10%
50V, $I_{DQ} = 100mA$
Integra 135W 3.1-3.5GHz
50Ω matched transistor

Typically 13dB gain, 50% efficiency, 10dB return loss

Typical application: phased array radar

Test Conditions:
300µs, 10%
46V, \( I_{\text{DQ}} = 25\text{mA} \)
100W CW 100-1000MHz GaN Pallet

Test Conditions:
\( V_{ds} = 28V \)
\( I_{DQ} = 480mA \)

Exploits low pF/W advantage of GaN
CONCLUSIONS

This paper has shown examples of state-of-the-art GaN products.