

RF Burn-in Analysis of 100V P-band Aerospace GaN Radar Transistors

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Abstract— Recent advances in solid-state amplifiers for aerospace applications have yielded GaN radar transistors operating at 75V and 100V in P-band with drain efficiency in the 80% range and output power of 250W and 500W. This study reports RF burn-in results at 100V and 125V bias with a signal at 430MHz, 100 μ s pulse width and 10% duty cycle to assess long term stability and reliability. With the test fixture kept at 26 °C the output power drops by ~2% at 100V and ~5% at 125V in a 1-week RF burn-in test. Measurements have been taken on GaN devices built on three different GaN on SiC epi configurations to determine the dependence of RF output power and gain degradation on properties such as iron (Fe) content in the epi buffer layer design. Results indicate that more stable operation with a bias of 100V and 125V is achieved when the Fe concentration in the buffer layer of the GaN device exceeds $1 \times 10^{18} \text{ cm}^{-3}$. Modeling of the thermal resistance under pulse conditions predicts a peak junction temperature of 84 °C at 125V bias when the test fixture is at 26 °C temperature, and it is 151 °C when the case temperature is increased to 80 °C. The result is significant because 28V and 50V commercially available GaN technology has already been proved to be tolerant to radiation suggesting that higher voltage GaN technology might be too. High voltage operation has the advantage of not only achieving higher power density and therefore smaller and lighter amplifiers but it also facilitates the implementation of harmonic tuning to obtain both very high efficiency and high output power, while reducing the requirements of the thermal cooling subsystem design. To the author's knowledge this is the first time that an RF radar amplifier has been tested for reliability at 125V with very promising results.

space applications. Compared to incumbent traveling-wave-tube (TWT) technology for space applications, solid-state power amplifiers have the benefit of potentially higher efficiency, smaller size and lower weight translating to lower cost in launching the spacecraft to orbit. Another advantage of solid-state power amplifiers is the much lower than kilo-volt range operating voltages which simplifies the design of the power supply subsystem. Given the limited prime power budget of a spacecraft, the efficiency of the radar front-end high power amplifier becomes a key element of the mission design. Therefore amplifiers for spaceborne applications are adopting GaN technology to achieve higher efficiency. For instance, harmonic tuning techniques were used in reference [3] to demonstrated 76% efficiency on a 10W GaN power amplifier at L-band, whereas in reference [4] the same approach was extended to a 100W single stage GaN amplifier to achieve 75% power added efficiency. Reference [5] reports on the application of such GaN technology for a 120W 2-stage amplifier module with 60% power added efficiency and 34dB power gain at L-band for SweepSAR radar systems. The design is based on state-of-the-art 50V GaN transistors made by Sumitomo Electric Device Innovations (SEDI) and matching networks optimized by active load-pull techniques at the fundamental frequency of 1.25GHz and the second harmonic [3]. System requirements call for 24 of these 100W modules to achieve a peak power in excess of 2kW, which translates into an overall power added efficiency that will be lower than 60% after combining losses. On the other hand, in reference [6] there is an analysis and comparison of class E, class F and inverse class F in L-band (2 GHz) to determine the best performance and trade-off achievable with a 10W GaN transistor. The 10W amplifier operation is targeted for satellite radio navigation applications (Galileo) and as such maximization of power added efficiency is the primary design objective in order to minimize DC power consumption, reduce self heating effects and improve overall reliability of the power amplifier. With that objective the authors conclude that class E mode of operation is the best compromise to achieve 75% power added efficiency at 10W output power. In reference [7] the typical performance goals of output power, bandwidth and overall efficiency are outlined for a T/R module in L-band for space needs. Here too the primary objective is the improvement achievable in the overall efficiency of the T/R module due to its implications on power consumption, thermal subsystem design, system reliability and overall cost of the mission. The authors describe a 30W power T/R module that achieves 70% overall efficiency at L-band (1250MHz) using

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1. INTRODUCTION

GaN HEMT technology has significant advantages in frequency band width, high voltage operation [1] and radiation hardness [2] that can be applied to high reliability

a push-pull class E/F circuit topology. In order to meet the 70% overall efficiency, the 30W power amplifier has 80% drain efficiency.

Besides L-band, several spaceborne applications exist in the UHF / P-band frequency range where GaN technology translates into significant advantages at the system level. The longer wavelengths of P-band are attractive since they can penetrate deeper into the ground, enabling new mission objectives such as subsurface radar imaging both for earth remote sensing and planetary space exploration. As discussed in reference [8], short wavelengths typical of L-band (1.2GHz, 24cm) can propagate through sand or sand-rich soil down to a depth of 1m to 2m, whereas the shorter wavelengths of C-band (6cm) and X-band (3cm) only propagate to shallower depths. The article discusses the benefits of using a multi-frequency multi-polarization radar system for revealing subsurface geology. A radar system designed to include P-band frequencies (440MHz, 68cm) allows deeper penetration through sand or any top layer of the surface crust. The radar system typically requires high output power (1-2kW) and as a spaceborne system high efficiency is mandatory to keep power supply requirements and weight manageable. An airborne test bed system for Biomass estimation (AirMOSS, Airborne Microwave Observatory of Subcanopy and Subsurface) is in operation using P-band SAR that is the precursor to future space instruments [9]. In reference [10] details of the NASA AirMOSS radar are discussed, with the P-band radar operating in the 280-440MHz frequency range, with a peak transmit power of 2kW. The system is actually based on the L-band radar (1.25GHz) used for the Uninhabited Aerial Vehicle Synthetic Aperture Radar (UAVSAR) with the addition of up and down frequency converters to convert the P-band signals to L-band and vice-versa. The UAVSAR radar produces a peak transmit power of 3.1kW, and uses a pulse length ranging from 2 to 50 μ s. The same pulse length is used for the AirMOSS radar. The system, built in 2006, is made of 24 T/R modules of 100W output power each, with a typical overall efficiency of 40% [11]. Compared to the L-band radar systems with 70% overall efficiency using GaN technology described above, there is a very good rationale and motivation for designing new radar systems in P-band with GaN technology and achieving state-of-the-art efficiency in excess of 60% or even 70%. For the BIOMASS mission [12] the European Space Agency (ESA) has funded development work for a high efficiency spaceborne power amplifier in P-band. The technical targets for this project are the following: narrow band from 432MHz to 438MHz with a pulse width up to 88 μ s and a pulse repetition frequency of 1.7 kHz, a large antenna of 11m-12m requiring a low average peak SAR power of 200W to 300W. Reference [13] reports on the 65% drain efficiency achieved at 180W output power using standard 50V GaN chips from two different vendors: UMS and Mitsubishi. The results are obtained in a switch-mode series tuned amplifier configuration which has the benefit of avoiding peak drain voltages that exceed the breakdown voltage of the device as could happen in pure class-E

amplification. It is noteworthy reporting that in order to avoid generation of spurious signals under load mismatch and ensure stability the GaN devices have to be operated at 40V bias. Another reason for operating the active device at reduced drain voltage is to meet ESA mandated 75% derating on electronics components used for space application. Also, the paper reports the trend of output power and efficiency versus drain bias. For both the UMS and the Mitsubishi devices, output power increases by 0.1dB per volt with higher drain voltage as expected but the efficiency quickly degrades by -0.75% per volt as the bias voltage is increased. The 50dB gain 150W peak power amplifier module with 65% added efficiency uses a 20mil thick pcb and is almost qualified having successfully completed multipaction tests [14].

In reference [15] the author of the present paper started investigating on a P-band high efficiency GaN-based power amplifier using switch mode techniques. A 24mm GaN on SiC HEMT transistor biased at 50V was used as a test vehicle to achieve the highest possible efficiency while using a switch-mode circuit topology. The single ended device achieved 150W output power with over 80% drain efficiency across the 420-450MHz bandwidth with a load matching network based on tuning of the 2nd and 3rd harmonics. This preliminary work was sponsored by an SBIR Phase I grant to Integra Technologies, Inc. and managed by NASA Jet Propulsion Laboratory (JPL). A follow-up SBIR Phase II grant awarded to Integra Technologies, Inc. made it possible continuing the research and development work where novel GaN on SiC HEMT transistors were designed and built. Such GaN technology has shown that higher voltage device operation at 75V and 100V combined with harmonic tuning techniques leads to single-chip transistor of 250W power output with over 80% drain efficiency in P-band [16]. Subsequent work has demonstrated a 500W single ended GaN transistor with 80% efficiency utilizing two power bars inside a single package operated at 75V as it will be reported in the next section. The final goal will be to scale the device up to a 1 kilo-watt peak power amplifier design that can be used for spacecraft radar applications requiring low power consumption. Also, the 100V device power bar has been utilized to explore pulsed operation at 125V at 430MHz with devices built on three different epitaxial designs featuring a different iron (Fe) concentration in the buffer layer of the device below the channel region. These results suggest that a minimum Fe concentration in the buffer layer of the GaN transistor is required to sustain reliable operation at enhanced bias operation of 100V or higher [17]. The primary goal of this article is to report RF burn-in test results conducted at 100V and 125V to assess in-the-field reliability of these high voltage GaN devices and to demonstrate that with the proper combination of epi, device design and high efficiency achieved through harmonic tuning reliable operation with GaN devices operated at 75V or higher is indeed possible. RF burn-in tests were conducted at 100V and 125V bias with a signal at 430MHz, 100 μ s pulse width and 10% duty cycle. The devices have 15mm gate periphery and achieve

output power of ~250W at 100V bias and >300W at 125V which translates into a power density of 17W/mm and >20W/mm, respectively. Initially the test fixture is kept at 26 °C by forced air cooling and the output power drops by ~2% at 100V and ~5% at 125V in a 1-week RF burn-in test. Most of the power drop occurs within the 1st and 2nd day, after which power versus time stabilizes. Next, the fan is removed and the test fixture temperature is allowed to increase to 47 °C at 100V and 57 °C at 125V bias. Output power drops by ~3.5% at 100V and ~7% at 125V due to the increase in junction temperature, whereas in the RF burn-in test following fan removal there is only negligible degradation as electrical stress has already occurred during the first segment of the RF burn-in test. We built GaN devices on three different GaN epi configurations varying the iron (Fe) content in the epi buffer layer. Results show that lower output power degradation is achieved when Fe concentration exceeds $1 \times 10^{18} \text{ cm}^{-3}$. Accurate modeling of the multi-layer structure thermal resistance has been used to predict the peak junction temperature under the pulse test conditions, which is 84 °C when the applied bias is 125V and forced air cooling keeps the test fixture at 26 °C, and it is 151 °C when the test fixture temperature is increased to 80 °C. The thermal model is calibrated against measured infrared imaging during the transient pulse on the 500W device operated at 75V. The result is significant because 28V and 50V commercially available GaN technology has already been proved to be tolerant to radiation with fluence of $1.6 \times 10^{12} \text{ proton/cm}^2$ at 55 MeV energy or heavy ions at several hundred MeV energy [2]. There is a very good rationale for believing that this higher voltage GaN technology is also radiation tolerant, which makes it a preferred solution for several space applications, not just radar related. The author believes the results presented in this paper advance the state-of-the-art knowledge in the field of high-efficiency high-power T/R modules for spaceborne applications, with possible application to airborne radars used in unmanned aerial systems (UAS) and ground-based radar systems as well.

2. HIGH VOLTAGE GAN SPACE TECHNOLOGY

Two families of high voltage GaN devices have been designed and analyzed: 1) a 21mm GaN on SiC HEMT transistor targeted to operate at 75V bias with a breakdown voltage in the 260V – 390V range depending on Fe content in the buffer layer; 2) a 15mm GaN on SiC HEMT transistor targeted to operate at 100V or higher with breakdown voltage from 430V to 610V depending on the Fe content in the buffer layer. Although having a different gate periphery, the two devices yield a similar output power of 250W [16]. A drawing of the 75V transistor layout is shown in Figure 1. The 21mm die topology features 80 gates of 260 μm gate unit width and a unit cell pitch of 45 μm on a 154mil x 40mil die physical size. The layout drawing of the 100V device looks very similar however the device features 60 gates of

250 μm gate unit width and a unit cell pitch of 60 μm on the same 154mil x 40mil die physical size.

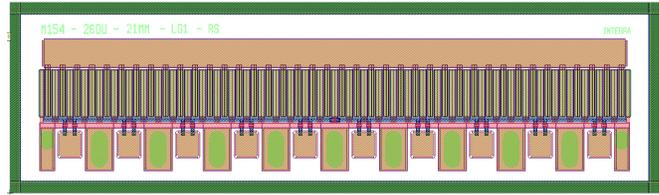


Figure 1. Layout drawing of the 75V GaN device.

The AlGaIn/GaN HEMT on SiC technology used in our research utilizes an epi structure consisting of a low temperature AlN nucleation layer on top of a semi-insulating SiC substrate, a 1.5 μm to 2 μm buffer layer Fe-doped away from the GaN channel region, the AlGaIn barrier, and a 3nm GaN cap layer. By varying the peak Fe concentration in the buffer layer the breakdown voltage of the transistor can be modulated from 260V to 390V for the 75V design and from 430V to 610V for the 100V design, as reported in more details in reference [17]. Using three different epi wafers, the Fe content in the buffer layer region away from the channel has been varied from a peak of $5 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$ and to $3 \times 10^{18} \text{ cm}^{-3}$. The AlGaIn/GaN HEMT device uses a well-established and mature fabrication process flow. Ohmic contacts are made of a Ti/Al/Ni/Au metal stack, annealed in a short and high-temperature rapid thermal annealing step. Ion-implantation is used for device isolation. Surface passivation is accomplished by PECVD low-stress silicon nitride deposition. For this project a 1 μm gate length shallow trench is formed by a low-damage silicon nitride etch step, followed by a 0.5 μm thick Ni/Au gate metal stack e-beam deposition that forms a gate overhang towards the drain for the gate-connected field plate. Another silicon nitride deposition step is used for isolation between the gate field plate and the next source-connected field plate. The second field plate layer is formed with another e-beam Au-based metal layer that also adds metal on top of the source and drain ohmic contacts for lower contact resistance. The final steps of the front-side process include the formation of air bridges and 3 μm thick plated Au for the source and drain fingers, as well as the wire bonding pads. To protect the chips from arcing effects due to high voltage metal lines exposed to air the chips are passivated with a 3 μm bisbenzocyclobutene (BCB) coating. Wafer processing is completed after back-grinding the SiC substrate to a 3-mil to 4-mil typical thickness and sputtered with TiAu back-metal. No back-via process is used on the wafers for the experiment reported in the present paper. The die is attached to the package flange with AuSn pre-form at 320 °C and the source pads are connected to the package flange through Au bond wires. The assembly configuration of two power bars inside the package is shown in Figure 2. This device achieves 500W output power with greater than 80% drain efficiency. In the case where a single power bar has been

used, exactly a half of what is shown in Figure 2 is included in the package; it is located at the center of the window frame and it achieves 250W saturated power. The ceramic package has a flange made of copper, molybdenum-copper alloy and copper (Cu/Mo70Cu/Cu, referred to as CPC) with thermal conductivity of 220 W/m-°K and 40-mil thickness. CPC is a sandwiched composite similar to Cu/Mo/Cu comprising a Mo70-Cu alloy core layer and two copper clad layers. The ratio of the thickness in Cu Mo70Cu and Cu layers is 1:4:1. Its thermal conductivity is higher than those of tungsten/copper (W/Cu), Mo/Cu, Cu/Mo/Cu and it is much cheaper. CPC flange based on molybdenum (Mo) and copper (Cu) alloy is also lighter compared to packages based on copper and tungsten (W) alloys and therefore preferable for aerospace applications. This package is also available in a hermetic solder seal for operation in harsh environment. The test device uses an input LC resonance to increase the input impedance of the die and the drain is bonded directly to the output transistor lead. Thick film series input resistors are used to enhance stability given the very high gain of the device when operated at 75V or 100V. Metalized substrates are also used on the input section so that longer wires can be used to achieve the required high inductance for a resonance at 430MHz. This direct bonding allows for fundamental and harmonic tuning outside the transistor package.

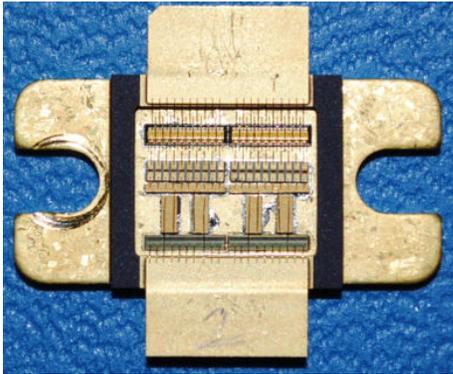


Figure 2. Assembly drawing of the device with two GaN chips positioned next to the output package lead (top side in the figure).

The series thick film chip resistors are positioned between the die gate pads and the LC section of the input pre-match. The test environment for the 500W device uses a test fixture with fixed tuned load impedances for all measurement frequencies with no external tuners. For the output match, the test circuit uses a drain bias line section adjusted in length to affect the impedances at the harmonics. The fundamental frequency is matched with shunt capacitors placed along a 50 ohm line at appropriate distances from the device to optimize the fundamental frequency load. For the input section, the fundamental frequency is also matched with shunt capacitors placed along a 50 ohm line at appropriate distances from the device. The load topology

might also benefit from effecting 4th and 5th order harmonics, but no measurements of impedance have been taken at those frequencies. A picture of the test fixture with the 500W device bolted down is reported in Figure 3.

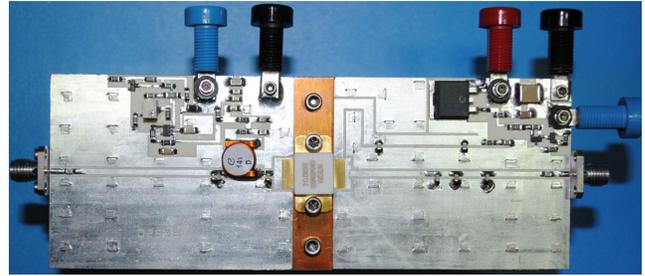


Figure 3. Picture of the Test Fixture and 500W device used for RF test at 75V bias.

The GaN device built with two power bars achieves a target of 500W output power and 80% drain efficiency across the 420MHz - 450MHz bandwidth. The configuration that has been selected for this test features two 21mm gate periphery chips operating at 75V. The device uses a pulsed waveform with 10% duty cycle and 300µs pulse width. Four samples of the 500W device were built and the performance was averaged for the data presented next. The quiescent current I_{DQ} was held constant over temperature and the gate-source voltage at quiescent current V_{GSQ} was adjusted at each temperature from 30 °C to 85 °C typical of the base plate temperature during operation. The fixture design used an estimate of optimum device impedance for the fundamental frequency match and empirically tuned harmonic elements to optimize efficiency. The fundamental frequency matching elements use a low pass structure with series transmission lines and shunt capacitance. The harmonic frequency matching uses open and short circuit transmission line shunt elements to reflect the harmonics back into the device. The electrical lengths of the transmission line elements were adjusted to optimize the amplifier efficiency. In doing so we implemented the principle according to which the number of harmonics determines the efficiency of the amplifier and the harmonics' impedances determine the output power capability of the device [18].

Table 1: Normalized Load Impedances for Class E, F and inverse F compared to measured data.

Freq	Class E	F	F ⁻¹	Normal. Z	Measured Z [Ω]
f_0	1+j0.725	1	1	1+j0.215	8.71+j1.87
$2f_0$	-j1.785	0	∞	0.051-j1.166	0.44-j10.16
$3f_0$	-j1.19	∞	0	0.006-j0.057	0.05-j0.495

Table 1 reports the measured impedances for the 500W amplifier at the fundamental, 2nd and 3rd harmonics de-embedded at the current-generator plane of reference, and compares the normalized impedance with the theoretical values that define pure class E, F and inverse F mode of operation as outlined in [18]. The measured data indicate that the 500W high efficiency amplifier is operating in a hybrid mode of operation which is a combination of the class E, F and inverse F.

Following is a plot of gain, drain efficiency and output power for the 500W device at 30°C base plate temperature and 450MHz operating frequency, shown in Figure 4. The 2x 21mm = 42mm device is biased at 75V with 80mA quiescent current (~2mA/mm). The linear gain is 24dB at an output power level of 100W. Also seen in Figure 4 is the peak drain efficiency of 81.2% reached at a 3dB compression point of 57.3dBm (537W) output power. Performance across frequency and temperature for the averaged data is presented for saturated power output and power gain in the next two graphs in Figures 5 and 6. Saturated power output is defined at 3dB gain compression from a gain reference at 100W. Increasing the temperature from 30 °C to 60 °C to 85 °C the saturated output power drops by ~30W at each step across the frequency range, corresponding to an average de-rating of 1W/°C. Under saturated power conditions the efficiency and pulse amplitude droop are shown in Figures 7 and 8.

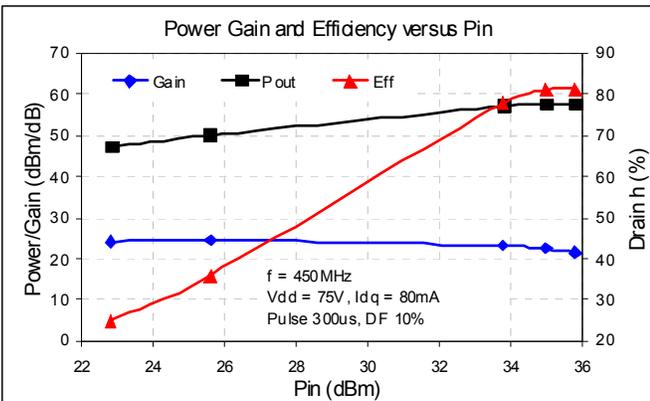


Figure 4. RF performance versus input power at 30°C base plate temperature and 450MHz. Pulse width is 300µs and the duty cycle is 10%. Bias voltage is 75V.

The drain efficiency is almost constant at ~81% across the 420-450MHz frequency range at 30 °C ambient temperature. It drops to ~79% as the baseplate temperature increases to 60 °C, and it drops further to ~77% when the temperature increases to 85 °C. On the other hand, the pulse droop is almost constant at -0.2dB across the temperature and frequency range. This result suggests that the efficiency drop over the case temperature range does not translate into a significant pulse distortion due to channel temperature.

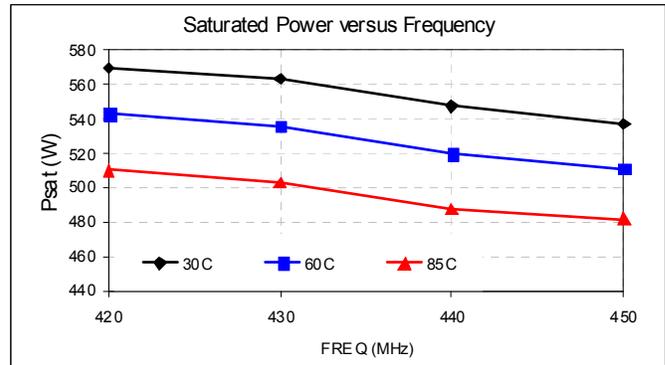


Figure 5. Saturated power versus frequency and case temperature. $V_{DD} = 75V$, $I_{DQ} = 80mA$; pulse width = 300µs, duty cycle = 10%.

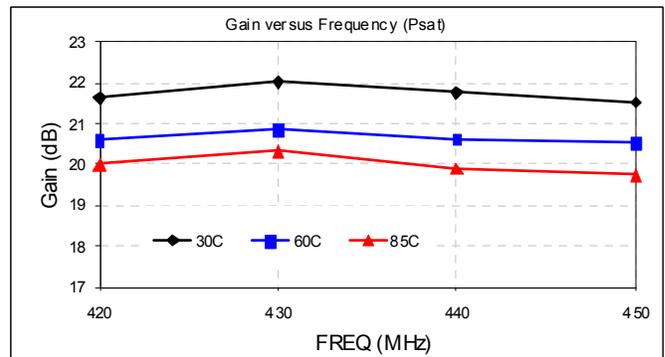


Figure 6. Gain at saturated power versus frequency and case temperature. $V_{DD} = 75V$, $I_{DQ} = 80mA$; pulse width = 300µs, duty cycle = 10%.

We also notice an almost linear power drop of 30W from 420MHz to 450MHz, independent of temperature, whereas power gain is almost constant across the band, but it does decrease by about 1dB for a 30 °C increase in the case temperature. The results presented here for the 500W device employing two power bars of 250W each establish a solid benchmark for the 75V GaN technology, but more data is necessary to determine its long term reliability. Therefore we have taken infrared thermal images of the 500W device to measure the channel temperature during a worst case scenario with 1ms 10% pulse and calibrate our thermal model, and looked back at the single power bars to undertake appropriate reliability analysis. The device built with a single power bar achieves a target of 250W output power and 80% drain efficiency across the 420MHz - 450MHz bandwidth. One configuration features a die of 21mm total gate periphery operating at 75V for a power density of 12W/mm; a second configuration features a die of 15mm total gate periphery operating at 100V for a power density of 17W/mm. Although both devices yield 250W output power, the 75V design easily reaches over 80% drain efficiency, whereas the 100V design could only achieve

75% drain efficiency. A more complete account of the results was published in reference [16].

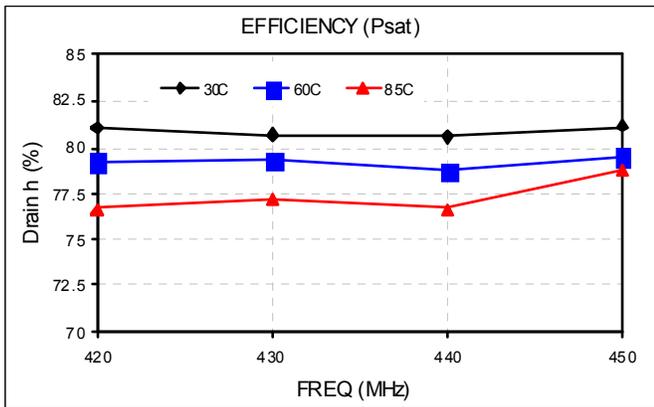


Figure 7. Drain efficiency at saturated power versus frequency and case temperature. $V_{DD} = 75V$, $I_{DQ} = 80mA$; pulse width = 300 μs , duty cycle = 10%.

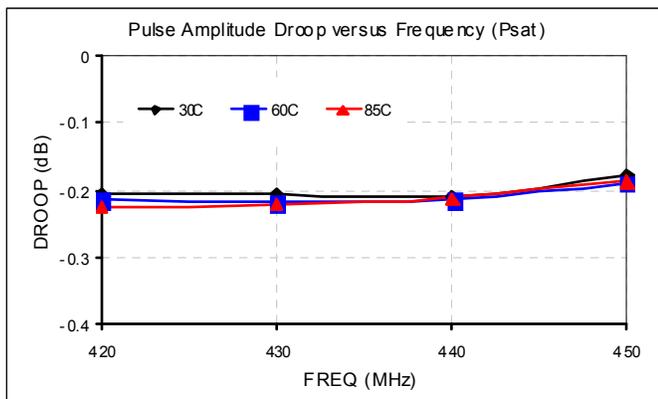


Figure 8. Pulse amplitude droop at saturated power versus frequency and case temperature. $V_{DD} = 75V$, $I_{DQ} = 80mA$; pulse width = 300 μs , duty cycle = 10%.

With a transistor operated at 100V and a power density of 17W/mm it is important to prove that the device is reliable enough to operate in the field with an acceptable lifetime. Between the 12W/mm design operated at 75V and the 17W/mm design operated at 100V we have chosen the more aggressive 100V design for reliability analysis. We have used a set of 100V devices for 1-week RF burn-in tests at 100V and 125V to gain insight into device design optimization from a reliability standpoint.

3. 100V P-BAND RF BURN-IN RESULTS

A first assessment level of device reliability is to stress the device electrically by operating it at increasing drain voltages; in our case it was used 75V, 100V, 125V and 150V. The same baseline test fixture, similar to the one

shown in Figure 3 has been used in all cases; in each measurement the device was matched for maximum output power with external slug tuners since the match was different at different bias. A cooling fan ensured the test fixture was kept at a temperature of 26 °C. A single power bar of the 15mm gate periphery die of 100V design was assembled in a ceramic package similar to what shown in Figure 2 and tested in a power amplifier at the single frequency of 430MHz. Three samples were tested each taken from a wafer with $5 \times 10^{17} \text{ cm}^{-3}$, $1 \times 10^{18} \text{ cm}^{-3}$ and $3 \times 10^{18} \text{ cm}^{-3}$ peak Fe concentration. RF data were collected on output power, drain efficiency and power gain. Each transistor is operated successively at 75V, 100V, 125V and 150V bias in a power sweep with a pulsed signal of 100 μs length and 10% duty cycle. Using a pulsed signal helps keep the thermal effects negligible. The data were presented in ref. [17] in the contest of developing a UHF GaN radar technology capable of operating at 125V. Results have shown that RF data for the three device families are roughly identical at 75V and 100V bias. On the contrary, a well defined difference in maximum output power and drain efficiency is observed at 125V and 150V bias. Power gain and drain efficiency versus output power are presented in Figures 9 and 10 for the 125V and 150V bias condition only, respectively. The sample with peak Fe concentration of $5 \times 10^{17} \text{ cm}^{-3}$ tolerates very well operation up to 100V bias with saturated output power increasing from ~150W to ~240W when bias increases from 75V to 100V, just like for the samples with higher Fe content. When the bias is further increased to 125V and 150V, the saturated power increases only marginally to ~300W and ~325W respectively for the sample with $5 \times 10^{17} \text{ cm}^{-3}$ peak Fe concentration, whereas saturated output power increases to ~350W and ~450W on the samples with $1 \times 10^{18} \text{ cm}^{-3}$ and $3 \times 10^{18} \text{ cm}^{-3}$ peak Fe concentration. More information about this work can be found in reference [17]. The results of saturated output power versus drain bias and peak Fe content are summarized in Figure 11 which shows a clear departure at 125V and 150V from the linear trend observed at a bias lower than 100V.

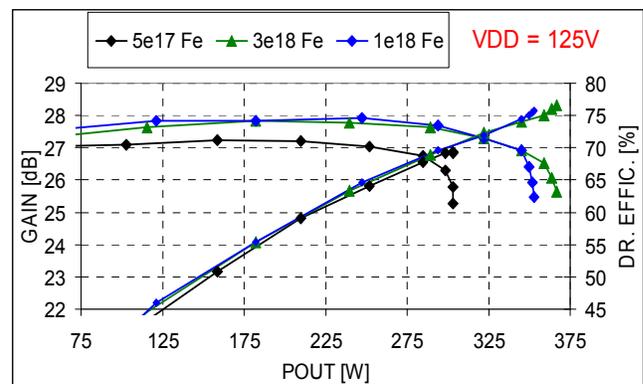


Figure 9. Gain and drain efficiency vs. output power drive-up at 430MHz for the 125V bias condition. Pulse length is 100 μs and duty factor is 10%.

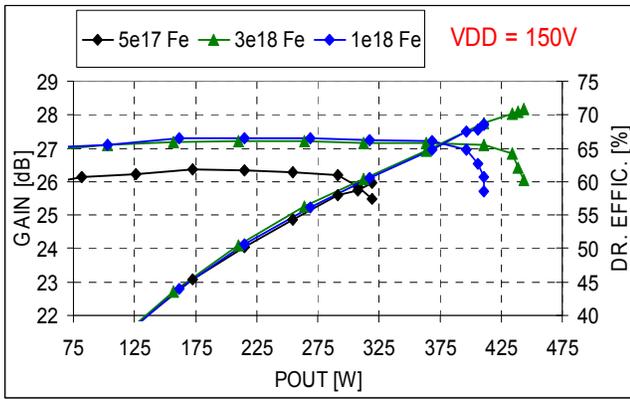


Figure 10. Gain and drain efficiency vs. output power drive-up at 430MHz for the 150V bias condition. Pulse length is 100µs and duty factor is 10%.

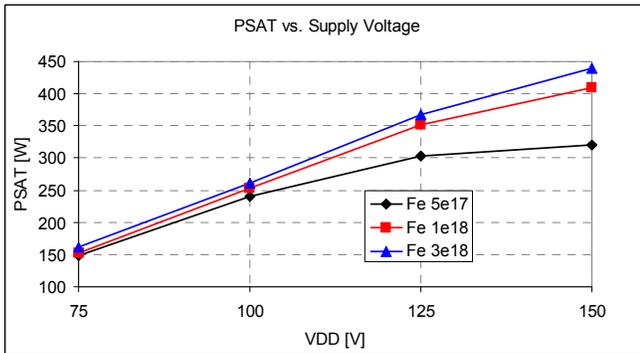


Figure 11. Saturated output power versus drain bias for wafers with different peak Fe content in the buffer layer.

At ~450W saturated power and 70% drain efficiency the 15mm device operated at 150V has an outstanding power density of 30W/mm, whereas at ~350W saturated power and 76% drain efficiency the same 15mm device operated at 125V has a power density of 23W/mm. With a transistor operated at 125V and a power density of 23W/mm it is important to prove that the device is reliable enough to operate in the field with an acceptable lifetime. A reliability analysis has been conducted by doing 1-week RF burn-in at ambient temperature, with the test fixture under forced air cooling at a temperature of 26 °C.

In Figure 12 we show variations of RF output power in percentage and gain reduction in dB at 100V for the three samples utilized in our electrical overstress work described above. Obviously the two sets of data for each device are proportional to each other. Results show that degradation in power and gain after a week operation is relatively small; from ~1% to 2%. Most of the degradation occurs during the first couple of days. The most striking result is the fact that the samples with higher peak Fe concentration in the buffer layer exhibit lower degradation. Next we subject the same

three devices to a 1-week RF burn-in at 125V bias and the data are reported in Figure 13. The devices continue to degrade with a reduction in power from 2% to 5%. Once again the most striking result is the fact that the samples with higher peak Fe concentration in the buffer layer exhibit lower degradation. At this point the cooling fan was switched off to let the device operate at increased temperature of the test fixture and therefore at increased junction temperature. The only cooling was provided by the air conditioning in the lab room. In Figure 14 the percentage of output power reduction from the starting value is shown versus time along with the test fixture temperature measured at the copper insert where the package is bolted down. Bias is 125V. In this test we notice both devices exhibiting output power reduction, but that is due to the increased channel temperature resulting from the increased case temperature to a range from 55°C - 60°C. Notice that once the case temperature stabilizes so does the output power indicating that these devices also achieve stable operation at increased case temperature.

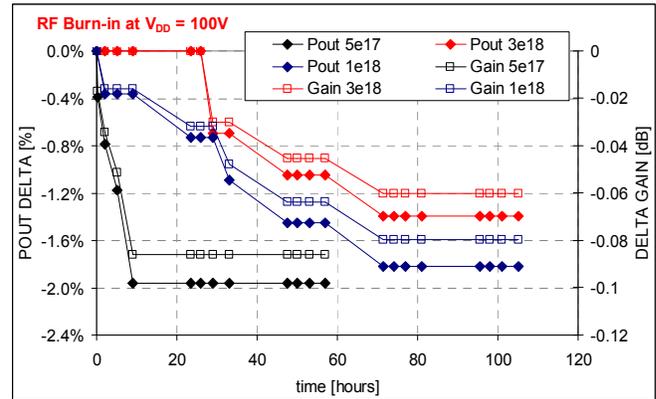


Figure 12. Gain and output power variation at 100V during RF burn-in: same devices after RF test at 150V.

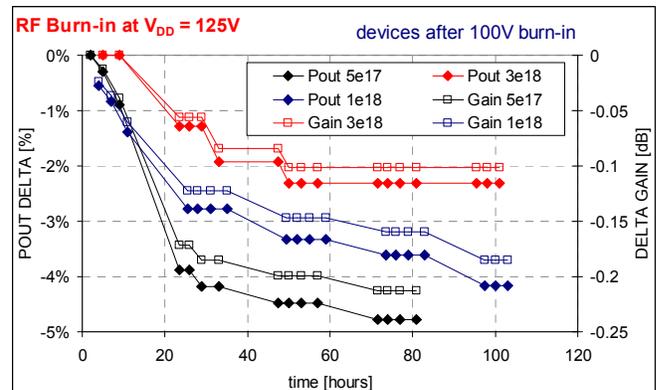


Figure 13. Gain and output power variation at 125V during RF burn-in: same devices after RF burn-in test at 100V.

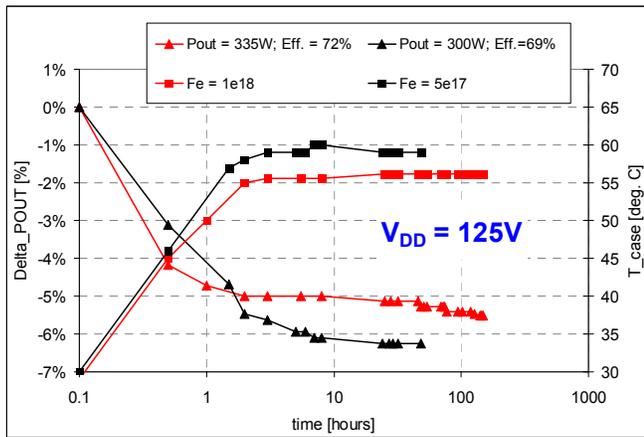


Figure 14. Output power variation at 125V and test fixture temperature versus time for two high voltage GaN transistors having $5 \times 10^{17} \text{ cm}^{-3}$ and $1 \times 10^{18} \text{ cm}^{-3}$ peak Fe concentration in the buffer layer.

After all, degradation due to RF burn-in has largely already occurred in the initial test at 26°C. Once the cooling fan was switched on again and the case temperature returned to ~26°C the output power for each part increased back toward the starting point. Last we took three virgin samples and subject them to a 1-week RF burn-in at 125V; the data are reported in Figure 15. In this case the power degradation is larger, ranging from ~4% for the samples with $1 \times 10^{18} \text{ cm}^{-3}$ and $3 \times 10^{18} \text{ cm}^{-3}$ peak Fe sample to ~6% for the sample with $5 \times 10^{17} \text{ cm}^{-3}$ peak Fe concentration. Here too most of the power reduction occurs with the first 24 to 48 hours, while it tends to stabilize afterwards. Next we took the better of these three devices with a $3 \times 10^{18} \text{ cm}^{-3}$ peak Fe concentration and increased test fixture temperature to 80°C and continue the RF burn-in for another week. This is different from the test whose data are reported in Figure 14 since by removing the cooling fan next to the test fixture would only increase the case temperature to a 55°C to 60°C range (45°C to 50°C range if bias is 100V). In Figure 16 the same output power and gain variations data are compared between the test fixture temperature at 26°C and at 80°C. Notice that there is an immediate power reduction of 5% which is due to the case temperature increasing from 26°C to 80°C, and once the set temperature of 80°C is reached the output power of the device stabilizes at 303W from the 320W measured at 26°C at the beginning of the test. After the initial transient the device operates flawlessly at 125V and 80°C case temperature. By comparing the three data sets we can extrapolate that a virgin device with peak Fe concentration equal to or higher than $1 \times 10^{18} \text{ cm}^{-3}$ operated at 100V would exhibit a power degradation of ~1.5% or less than 0.1dB reduction in an RF burn-in test at room temperature which is totally acceptable from a system reliability standpoint. No RF burn-in tests have been conducted on the 21mm devices operated at 75V since there is a limited supply of 75V devices which need to be spared for continuing research work on the 1 kilowatt power amplifier module. With a

lower power density and higher efficiency compared to the 100V devices we now have enough information to make an informed guess that these devices in a similar RF burn-in test would yield output power degradation smaller than 1%.

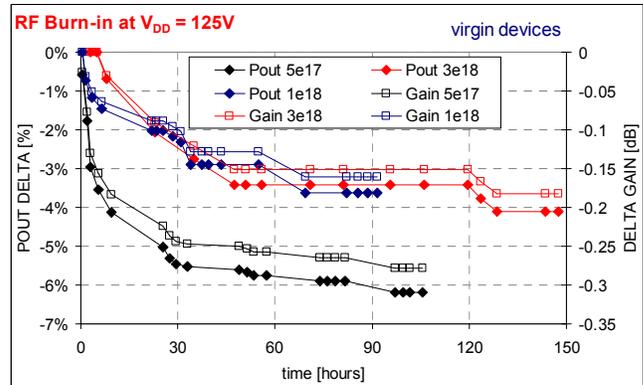


Figure 15. Gain and output power variation at 125V during RF burn-in: virgin devices.

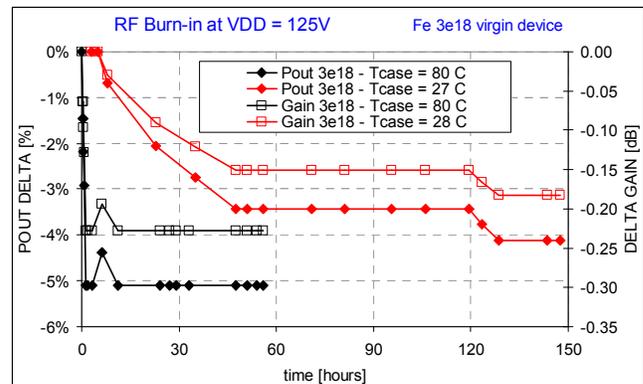


Figure 16. Gain and output power variation at 125V during RF burn-in for a virgin device with $3 \times 10^{18} \text{ cm}^{-3}$ peak Fe concentration at 27°C and successively repeated at 80°C.

The ultimate question still unanswered is what the cause of the power degradation is. For example, early LDMOS devices had to be burnt-in due to the drift of threshold voltage with time. This had a very serious effect on the linearity of the device with the linearity changing with time due to the shift of threshold voltage and hence the quiescent current I_{DQ} . Also, is the change permanent or reversible? For example, VDMOS output power degrades with time but the change is reversible by baking the device in an oven for a few hours with no applied bias. In the case of VDMOS the degradation in power is caused by hot electrons getting injected into the oxide layer and putting a charge which causes a pinch-off of the channel region and reduces the maximum saturated drain current and hence output power.

Is a similar effect happening with these GaN devices? Given that Figure 12 shows some definite correlation between degradation and Fe concentration in the buffer layer, this suggests that the degradation might be related to the gradual annealing of stress at the interface between the buffer and epi layer. Another potential ambiguity is in how to interpret the RF burn-in tests. For instance, it is possible that the data show that the higher Fe concentration parts degrade less, but it is also possible that the time constant for the degradation differs markedly with Fe concentration, as Figure 12 could suggest. The question then is why does Fe concentration alter the time constant? The higher Fe concentration parts would need to be run for much longer to see if they have really stabilized before being able to state categorically that they degrade less. However, Figure 12 shows RF burn-in data at 100V bias and at 100V or lower voltage the data reported in this work and in ref. [17] show that not much difference is observed when Fe content is varied. It is only when bias increases above 100V where differences due to Fe content start manifesting themselves as Figure 11 explicitly indicates. There has been significant reliability data published on standard 50V GaN technology and nowadays 50V GaN technology is considered reliable enough for several applications on Earth and qualified for spaceborne applications as well. To the author's knowledge, this work is the first report on reliability of GaN technology operated from 75V to 125V and there is definitely room for additional reliability work to be done in the future. At this time, in order to further understand the implications of these electrical over-stress and RF burn-in tests we have used a compact model to simulate the junction or channel temperature of the device while in operation. We plan on comparing junction temperature data for the 100V devices we have taken RF burn-in tests on with the 75V devices which we have not tested.

4. JUNCTION TEMPERATURE MODELING

Thermal imaging data were collected on the 21mm 75V GaN HEMT transistor die to understand limitations and margins for reliable operation. The infrared thermal measurement data were taken at Quantum Focus Instruments Corporation (QFI) in Vista, California using the InfraScope™ Temperature Mapping Microscope with a 3 μ m spatial resolution. The test conditions for the devices used 80°C base plate temperature, 450MHz operating frequency under pulse waveforms of 100 μ s, 300 μ s and 1ms with 10% duty cycle. During the thermal measurement RF output power was set to levels near the saturated power of the devices. Figure 17 below shows the thermal image of the 21mm 75V die under 100 μ s pulse and 10% duty cycle. Thermal image of the copper heat spreader adjacent to the device package showed a base plate temperature of 81°C. The average output power is 23W (230W peak pulse power) per individual die, dissipated power is 7W per each die and the average peak temperature in the thermal image is 98°C corresponding to a temperature increase of 17°C and a thermal resistance of 2.4 °C/W. The peak temperature is

measured on a 3 μ m pixel resolution. If the average temperature profile is smoothed on a 15 μ m resolution the peak temperature is 3.5°C lower and this offset is used to extract the equivalent peak temperature during the transient pulse because the transient detector has only 15 μ m spatial resolution.

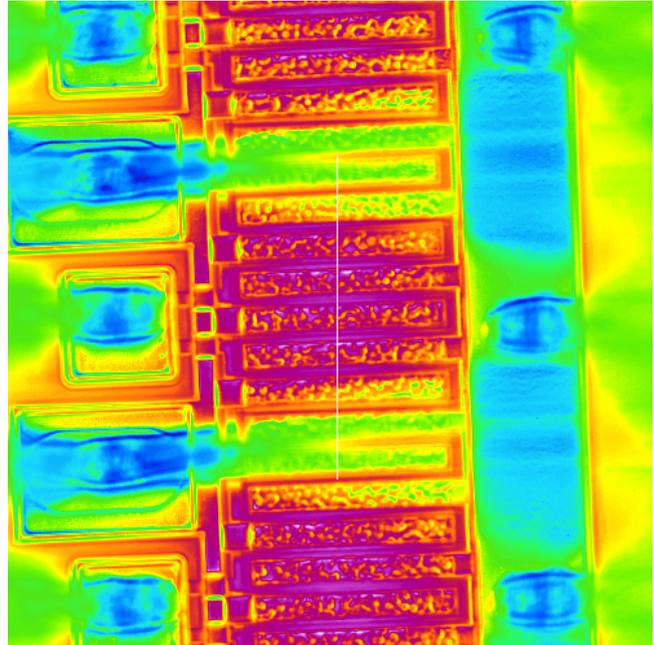


Figure 17. Thermal image of the 75V during RF operation with the base plate temperature at 80°C. The measured die peak temperature in red color is 98°C on a spatial resolution of 3 μ m. Pulse condition for this test is 100 μ s and 10% duty cycle.

From reliability perspective more interesting is to measure the peak temperature during the transient pulse and not the average, which is measured with a Transient High Speed Thermal detector with a bandwidth of 240 kHz capable of resolving a temperature transient of 4 μ s – 5 μ s length. The transient thermal detector has a spatial resolution of 15 μ m. In Figure 18 the temperature profile during a pulse of 1ms period and 10% duty factor is shown. The measured peak temperature captured by the ultra-fast response detector on a 15 μ m spatial resolution is 154.6°C; by adding the 3.5°C resolution corrective factor the estimated peak temperature during the 1ms 10% pulse is 158.1°C yielding an effective thermal resistance of 0.99°C/W.

A thermal simulation model has been used next to reproduce the measured data for the 21mm device and calibrate the model. Considering the importance of the junction temperature on the reliability of the device, several methods and techniques have been used to improve the accuracy of peak junction temperature modeling near the gate of the

transistor. In reference [19] a finite element method is discussed that includes effects from the package, die-attach solder, SiC substrate and thin GaN epi-layer regions that make up the device and each adds its component to the total thermal resistance. The method also adds spatial averaging techniques that allow matching simulated to measured data and the agreement is very good.

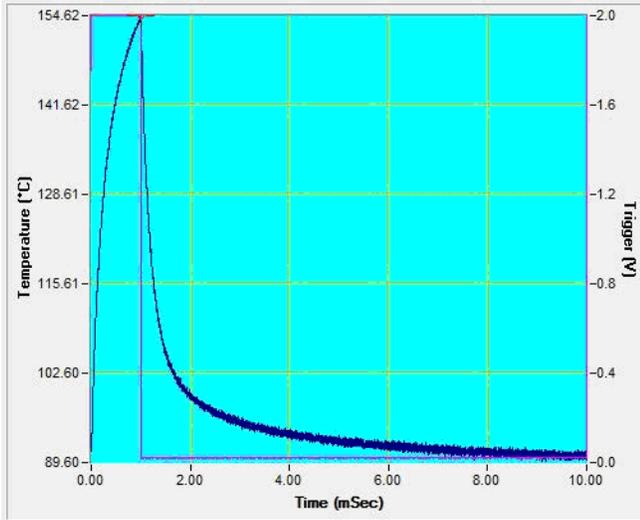


Figure 18. 75V die transient channel temperature profile during RF operation with the base plate temperature at 80°C. Pulse condition for this test is 1ms and 10% duty cycle. Peak channel temperature is 154.6°C on a 15 μ m spatial resolution when output power is 225W per die, dissipated power is 78W.

Unfortunately this method is computationally intensive and it would be impractical using it for designing new chip designs or analyze a given device under different bias or pulse conditions such as is done in our work. Therefore a compact model that could yield the calculation of the peak temperature in the channel region of the device with sufficient accuracy is highly desirable. An excellent solution has been provided in reference [20]. The model includes temperature dependence in the thermal conductivity of the material, and accounts for die attach substrate and GaN layers. We have also included the element due to the package by using a model similar to what is used in [20] for the die attach layer; the flange thickness is 40mil and we have used the die area for the effective area of the package rather than the area of the window frame. Then we have computed the temperature variation in the package, die-attach, SiC substrate and GaN layers where each layer uses the temperature calculated at the bottom interface, as explained in [20]. For the GaN material at $T = 300$ °K we have used the thermal conductivity of 165 W/m $^{\circ}$ K as used in [20]; however there have been recent measurements based on the micro-Raman scattering technique where the

measured value is closer to 200 W/m $^{\circ}$ K, as reported recently in [21]. Interestingly enough, only minor dependence of this value on carbon and iron doping was reported. Reference [19] used a value of 130 W/m $^{\circ}$ K for the GaN layer thermal conductivity at 300 °K. Our choice of 165 W/m $^{\circ}$ K is therefore a compromise between what other researchers have been using in the literature and what the latest measurements indicate. Furthermore, the model has been adapted to transient analysis under the 100 μ s, 300 μ s and 1ms pulse width and 10% duty cycle used in this work. Values for density and specific heat of the different material layers to calculate the thermal capacitance have been taken from table 2 in reference [19]. Figure 19 shows a circuit schematic of the thermal model as implemented in a SPICE simulator for the transient analysis whereas in Table 2 we show the calculated values for thermal capacitance and resistance of each layer in the modeled structure. We have assumed a perfect thermal interface between the bottom of the package flange and the copper base plate. The modeled profile of the temperature pulse agrees pretty well with the measured data, yielding a peak temperature of 157 °C and an effective thermal resistance of 0.98 °C/W.

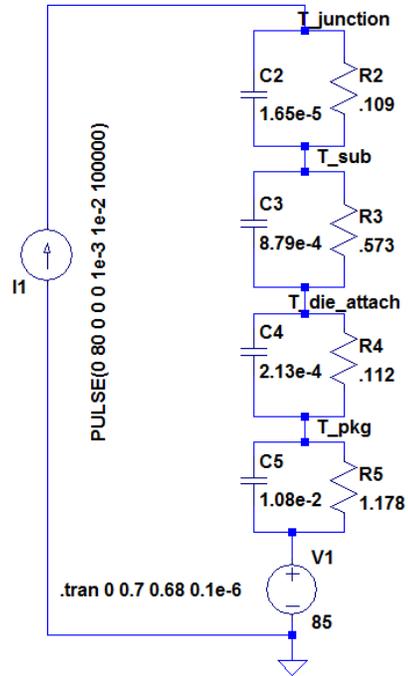


Figure 19. Thermal transient model of the 75V, 21mm device with case at 85 °C and dissipated power of 78W.

Based on the good agreement between available measured thermal data and the modeled results presented in this section, we have used the model to analyze the thermal behavior of this same die under more typical signal pulse conditions used in a remote-sensing SAR system such as

300 μ s and 100 μ s pulse with 10% duty cycle with maximum case temperature of 80 °C, and then we turn our attention in modeling the thermal behavior of the 100V devices we have characterized in the RF burn-in tests presented earlier.

Table 2: Calculated thermal capacitance and resistance for the four layers in the modeled structure of the 75V, 21mm die with case temperature at 85 °C and dissipated power of 78W as measured at Quantum Focus Instr.

Layer	Thickness [μ m]	Area [mil ²]	C_{TH} [J/°K]	R_{TH} [°K/W] $T_{case} = 85\text{ °C}$
GaN epi	2	152 x 40	1.65×10^{-5}	0.109
SiC substr.	75	152 x 40	8.79×10^{-4}	0.573
AuSn solder	25	152 x 40	2.13×10^{-4}	0.112
CPC Pkg.	1016	152 x 40	1.08×10^{-2}	1.178

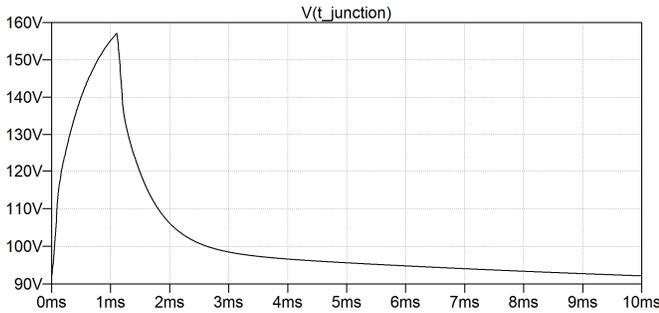


Figure 20. Simulated transient channel temperature for the 75V, 21mm device with case at 85 °C and dissipated power of 78W with 1ms 10% pulse as measured at Quantum Focus Instrument Corp. Peak temperature is 157 °C for an effective thermal resistance of 0.98 °C/W.

Looking back at the data in Figures 5 and 7 at 450MHz the 2-chip device at 75V under 300 μ s 10% pulse with 80°C (30°C) base plate temperature yields 480W (540W) saturated output power and 78% (81%) drain efficiency; therefore the DC power is $480W / 0.78 = 615W$ ($540W / 0.81 = 667W$), and the dissipated power is $615W - 480W = 135W$ ($667W - 540W = 127W$) for the two chips, or 68W (63.5W) in each chip. Table 3 reports the calculated components for the thermal capacitance and thermal resistance of each layer which is slightly different for the transistor layers when the case temperature is 30°C and 85°C. Since the die size is unchanged compared to Table 2, the column has been removed here. The peak junction temperature is 127.8 °C with the case temperature at 85°C corresponding to a thermal resistance of 0.63 °C/W; it is 67 °C when the case is at 30 °C and the thermal resistance is 0.58 °C/W. The respective temperature pulse train profiles are reported in Figures 21 and 22.

Table 3: Calculated thermal capacitance and resistance for the four layers in the modeled structure of the 75V, 21mm die with case temperature at 85 °C and 30 °C with 300 μ s pulse and 10% duty cycle.

Layer	Thickness [μ m]	C_{TH} [J/°K]	R_{TH} [°K/W] $T_{case} = 30\text{ °C}$	R_{TH} [°K/W] $T_{case} = 85\text{ °C}$
GaN epi	2	1.65×10^{-5}	0.097	0.109
SiC substr.	75	8.79×10^{-4}	0.375	0.569
AuSn solder	25	2.13×10^{-4}	0.112	0.112
CPC Pkg.	1016	1.08×10^{-2}	1.178	1.178

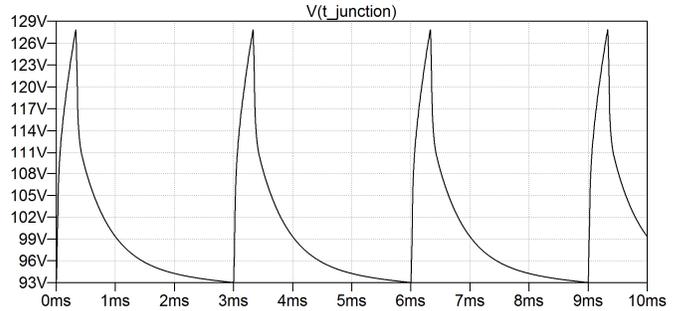


Figure 21. Simulated transient channel temperature for the 75V 21mm device with case at 85 °C and dissipated power of 68W. Pulse width is 300 μ s and duty cycle 10%. Peak temperature is 127.8 °C for an effective thermal resistance of 0.63 °C/W.

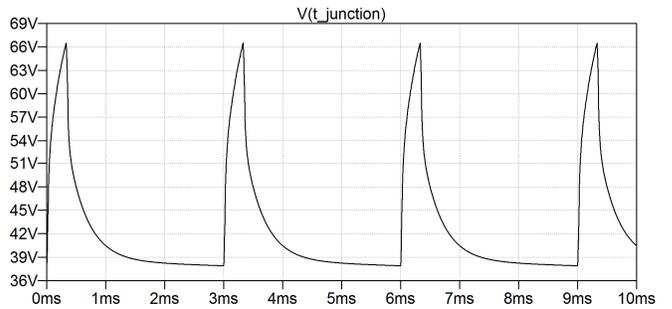


Figure 22. Simulated transient channel temperature for the 75V, 21mm device with case at 30 °C and dissipated power of 63.7W with 300 μ s 10% pulse. Peak channel temperature is 67 °C for an effective thermal resistance of 0.58 °C/W.

Based on the simulated junction temperature of the 500W device with 300 μ s 10% pulse we conclude that the device operates in a safe region. Pulse width for spaceborne SAR systems is typically shorter than 100 μ s and the duty cycle shorter than 10%, further lowering the peak junction temperature during operation. Next we apply the same thermal model to the 15mm 100V die design to model temperature junction profile with a case temperature of

26°C and 80°C when the device is operated at 125V. In this case the pulse is 100µs wide and the duty cycle is 10%. Measured RF data at 430MHz for the device at 125V yield 350W output power and 76% drain efficiency with the peak drain current at 3.7A; therefore the DC power is 3.7A x 125V = 460W (or 350W / 76% = 460W), and the dissipated power is 460W - 350W = 110W. The GaN die has the same size of 152mil x 40 mil, and we have used the die area as the effective area of the package. The model of the package yields an R_{TH} of 1.178 °C/W. For die attach we have used AuSn with 25µm thickness, as the pre-form sheet is 1-mil thick. Its thermal resistance is 0.112 °C/W. So far the model is essentially unchanged compared to the 21mm die of 75V. Including the nonlinearity of the SiC substrate and GaN epi-layer (~2µm thick) thermal conductivity, their calculated thermal resistances are 0.603 and 0.148 °C/W respectively when the base-plate temperature is 26 °C under forced air cooling. Furthermore, the model has been adapted to transient analysis under the 100µs pulse width and 10% duty cycle used in this part of the work. Values for density and specific heat of the different material layers to calculate the thermal capacitance have been taken from reference [19], table 2. The junction temperature with 110W dissipated power during the 100µs pulse reaches a peak value of 84 °C which is conducive to high reliability operation. The transient junction temperature plot is shown in Figure 23.

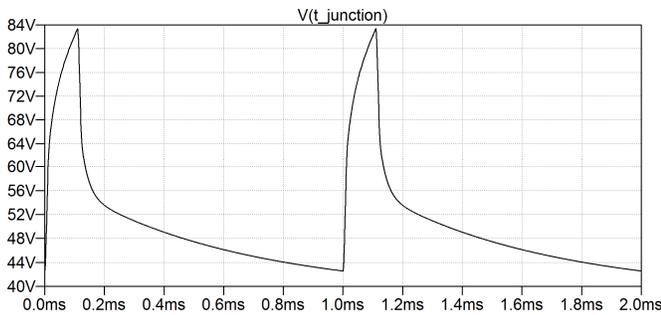


Figure 23. Simulated transient channel temperature for the 15mm 100V design; the device is operated at 125V with base plate at 26 °C and dissipated power of 110W under 100µs 10% pulse conditions. Peak temperature is 84 °C for an effective thermal resistance of 0.53 °C/W.

When the base plate temperature is increased to 80 °C the output power drops and so does the efficiency; in the RF burn-in test we reported in Figure 16 the output power sets at 303W with 70% efficiency. That translates into a dissipated power of 303W / 0.7 = 433W and the dissipated power is 433W - 303W = 130W. In this case the model of the package that houses the 15mm GaN chip yields again an R_{TH} of 1.178 °C/W since the thermal conductivity of the CPC flange has been assumed temperature independent. The die attach AuSn layer has again 25µm thickness, as the pre-

form sheet is 1-mil thick. Its thermal resistance is again 0.112 °C/W. Including the nonlinearity of the SiC substrate and GaN epi-layer (~2µm thick) thermal conductivity, their calculated thermal resistances are now 0.743 and 0.156 °C/W respectively. Therefore the total thermal resistance under CW conditions would be 2.19 °C/W. However, the junction temperature with 130W dissipated power during the 100µs pulse reaches a peak value of 151 °C which is comparable to the channel temperature of the 500W device operated at 75V with 1ms pulse length and it is definitely acceptable for high reliability operation. The transient junction temperature plot in this case is shown in Figure 24 and Table 4 summarizes the thermal capacitance and resistance of each layer in the model of the 100V design operated at 125V at 26 °C and 80 °C base plate temperature.

Table 4: Calculated thermal capacitance and resistance for the four layers of the modeled structure. Due to nonlinear thermal conductivity of SiC substrate and GaN epitaxial layer, the computed thermal resistance is different when the case temperature is 26 °C or 80 °C, hence two columns are provided.

Layer	Thickness [µm]	Area [mil ²]	C_{TH} [J/K]	R_{TH} [°K/W] $T_{case} = 26 °C$	R_{TH} [°K/W] $T_{case} = 80 °C$
GaN epi	2	152 x 40	1.65×10^{-5}	0.148	0.156
SiC substr.	75	152 x 40	8.79×10^{-4}	0.603	0.743
AuSn solder	25	152 x 40	2.13×10^{-4}	0.112	0.112
CPC Pkg.	1016	152 x 40	1.08×10^{-2}	1.178	1.178

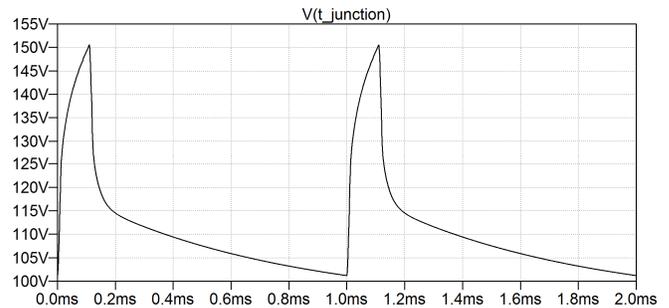


Figure 24. Simulated transient channel temperature for the 15mm 100V design; the device is operated at 125V with base plate at 80 °C and dissipated power of 130W under 100µs 10% pulse conditions. Peak temperature is 151 °C for an effective thermal resistance of 0.55 °C/W.

Before closing this section a final comment is required to explore the possibility of using this high voltage GaN technology with CW signal for potential applications in CW radar or even communication links. With a CW thermal resistance around 2 °C/W and typical maximum base plate junction around 80 °C, in order to keep the peak junction

temperature below 200 °C the dissipated power in each die should be limited to 50W or 60W at most. That can be accomplished by either reducing the gate periphery of the die to 10mm range or operating the device at 100V rather than 125V, or a combination of both. For example, the 15mm device tested in this paper at 125V with output power greater than 300W would only achieve ~250W at 100V bias in pulse conditions. CW operation also translates into a reduced power density to ~200W saturated power. With harmonic tuning the efficiency could be maintained in the 75% to 80% range and to get a ballpark figure we could use a conservative figure of 75%. In such conditions the dissipated power would be $200W / 0.75 = 267W$ which is not too far from the 50W – 60W limit range. By decreasing the die size to the 10mm to 12mm range the saturated output power would be in the 130W to 160W. With 160W saturated output power the math for dissipated power is now the following: $160W / 0.75 = 213W$ which is well within the feasibility territory. A final note about radiation hardness is also necessary. At this time no radiation tests have been done on these high voltage GaN transistor; however in reference [2] high dose proton and heavy ions damage tests are reported on commercially available 50V and 28V GaN technology. The results show that the GaN HEMT structure, due to its depletion mode nature and the wide band gap properties of the Gallium Nitride epi and semi-insulating Silicon Carbide substrate materials, is not impacted and it can tolerate high level of radiation as seen in space or in harsh environments on Earth. Although higher voltage operation in the GaN transistors studied in this work leads to a different electric field profile in the device, the depletion mode nature of the device and the material properties of the Gallium Nitride material are the same. It is therefore legitimate to assume that these high voltage devices are radiation tolerant as well, and further tests in the near future might actually validate this assumption.

5. SUMMARY

The development of a high voltage GaN technology suitable for spaceborne radar systems has been reported. A 500W radar transistor operating at 75V in P-band with 80% efficiency for spaceborne SAR applications has been described as a demonstration of the technology's capabilities. In particular, the paper addresses the reliability of this newly developed technology. RF burn-in tests have been done at 125V under various conditions on a device with a single die achieving >300W output power. Results show that the drop in output power is lower when the iron (Fe) concentration in the buffer layer of the transistor is at least $1 \times 10^{18} \text{ cm}^{-3}$. Furthermore, thermal imaging of the 500W device with 1ms 10% pulse shows a peak channel temperature of 158 °C which is very safe from a reliability perspective. A thermal model has been used to model the device thermal characteristic. After calibration, the model has been used to reveal the peak junction temperature of the device operated at 125V and the results show that at 80 °C

base plate temperature the channel reaches a peak of 151 °C. The results reported in this paper show that high voltage GaN technology can reliably operate in pulse power amplifiers for spaceborne applications. No data are available on radiation induced damage effects on high voltage GaN transistors, but the GaN on SiC HEMT transistor architecture has already been proved radiation tolerant on commercially available 50V GaN technology suggesting that the newly developed high voltage GaN technology could too. Last, a possible scenario on how to adapt this high voltage GaN technology to CW applications has been discussed. The author believes that the results presented in this work advance the state-of-the-art knowledge in the field of high-efficiency high-power amplifiers for spaceborne applications, with possible application to airborne, shipborne and ground-based radar systems at UHF or higher frequencies. The paper's main purpose is perhaps to prove that operating RF GaN transistors at higher voltage from 75V to 100V and 125V in UHF is soon to be a reality and the author hopes that the breadth of data presented in the paper suggests so.

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